PRM: collecting info from the HW point of view

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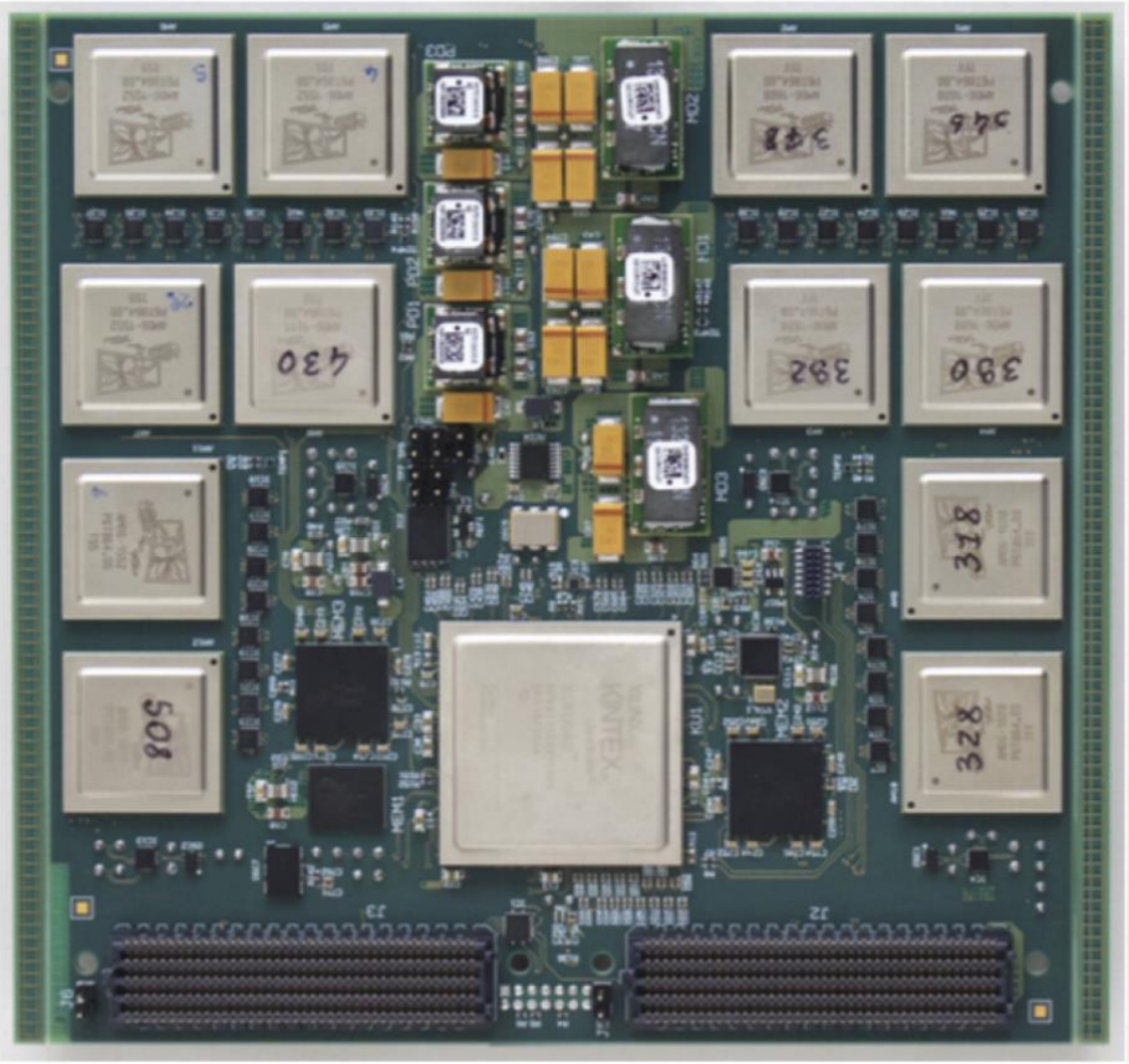
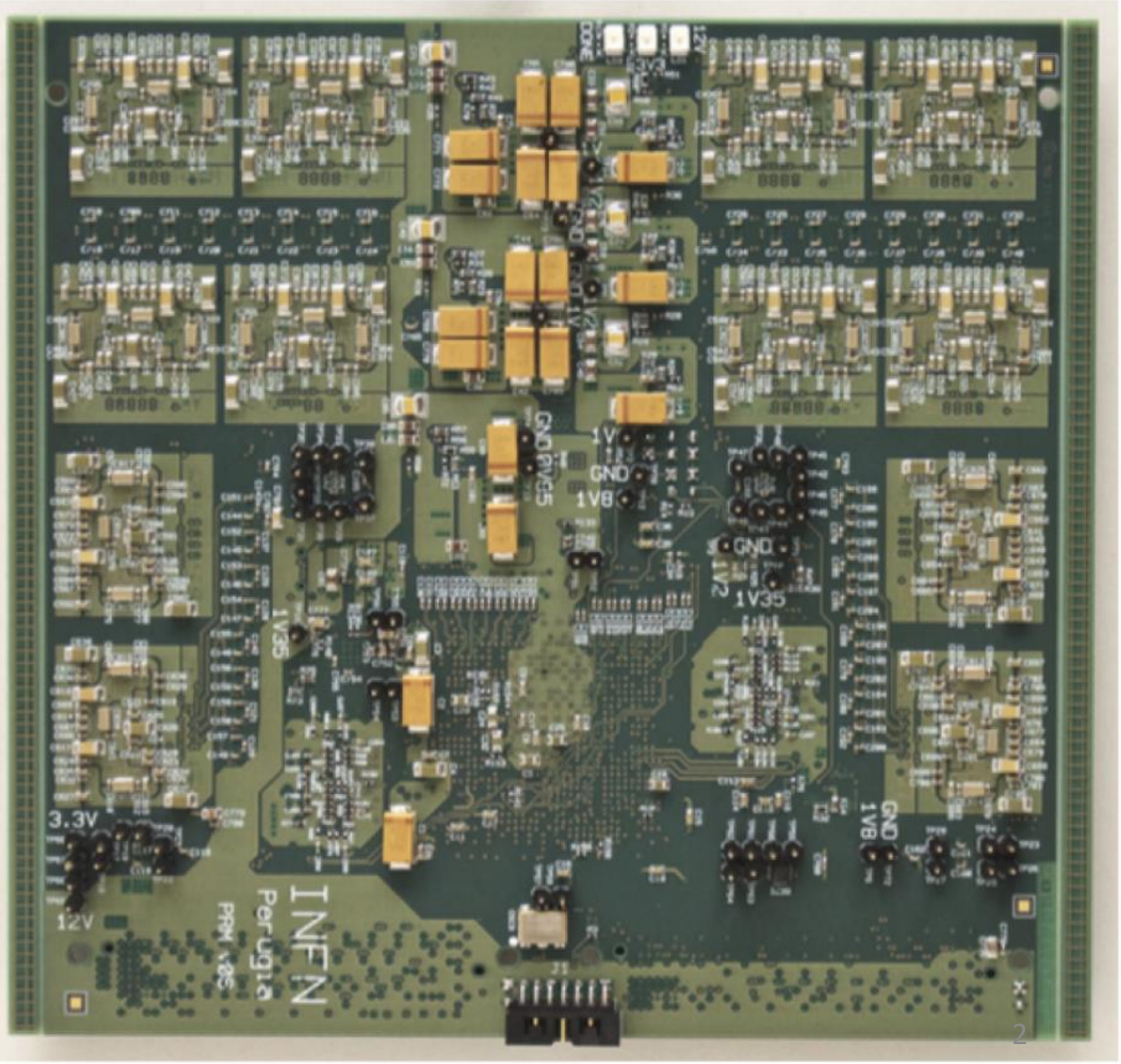
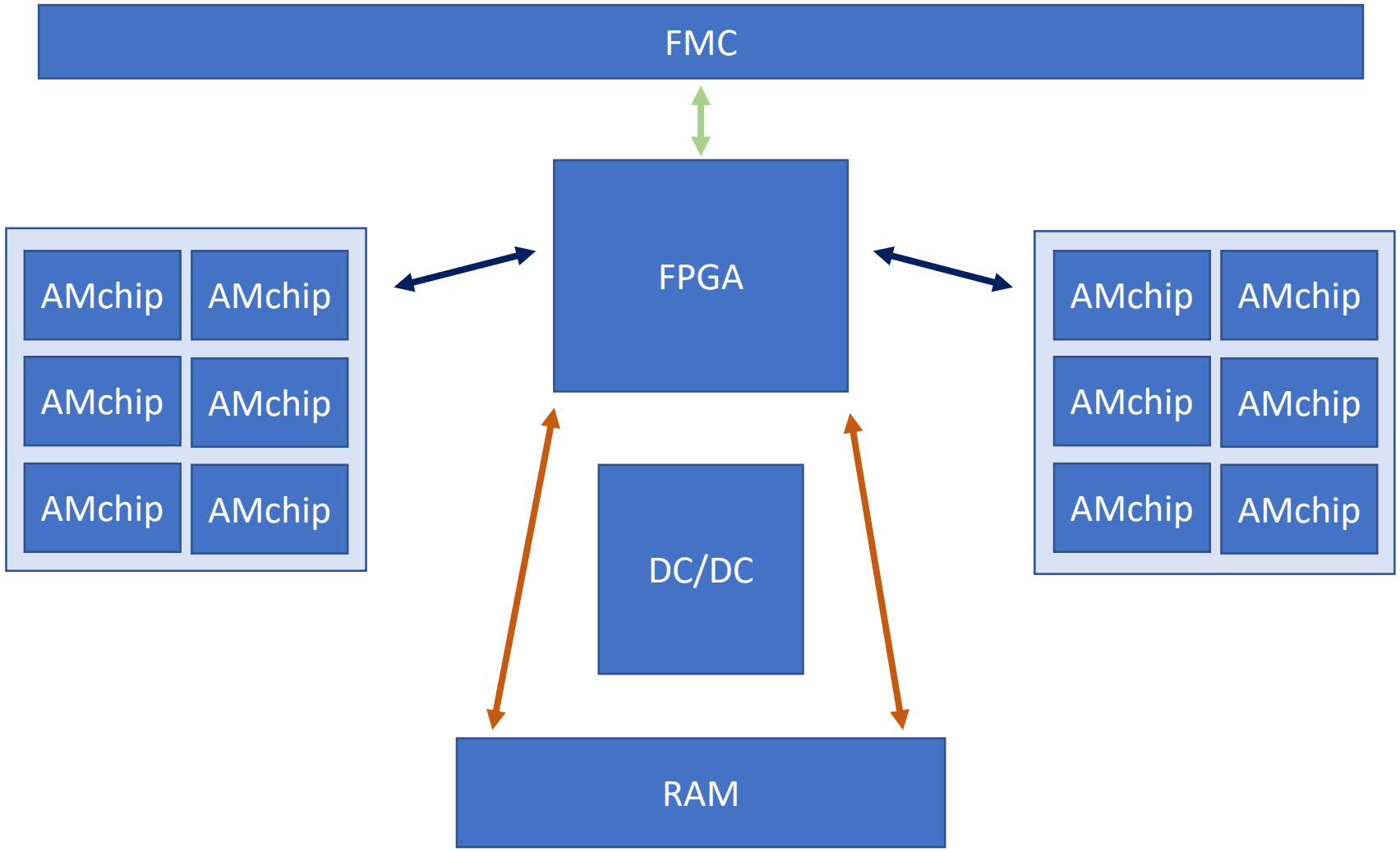
Old pre-prototype





Present idea

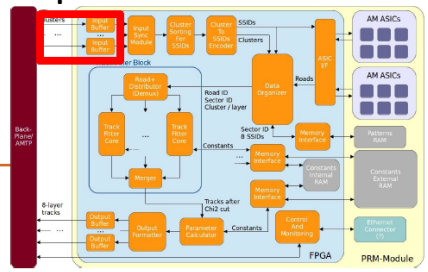


FPGA – FMC (green)

Assuming a maximum of 32 bits per cluster for L1 Track applications we can calculate that we require 8 layers x 32 bits x 2 groups of AM Chips = 128 Gb/s. We assume an overhead of 20% for packet words, protocol (e.g. 66/64), module headers etc. and therefore the required input speed is 128Gb/s x 1.2 = 160Gb/s. Therefore 16 high speed links are required at the input (10Gb/s per link) for L1, while we can consider that 8 high speed links are sufficient for L0.

PRM Input Interface - Data Flow

Input interface of the PRM FPGA



Block Name	Rate at Input (Required)	Input Format	Input Data	Output Format	Output Data	Output Time
Input Links/Buffers	160Gb/s	32 - 48 bit	Clusters	32 - 48 bit	Clusters	One Cluster per Clock

- **Rate at Input**
  - The Data Flow requirements are specified by the maximum operational speed of the AM Chips (250 MHz) for the requirements of L1 Track
  - 8 layers x 250 MHz x 32 bits x 2 groups of AM Chips = 128 Gb/s
    - Assume maximum 32 bits per cluster for L1 Track applications
  - 128 Gb/s x 1.2 (~20% overhead for packet words etc) = 160 Gb/s
    - 16 High speed Links (10Gb/s) 8 layers x 2 links for L1
    - 8 High speed Links are sufficient for L0

FMC connectors

Tensions

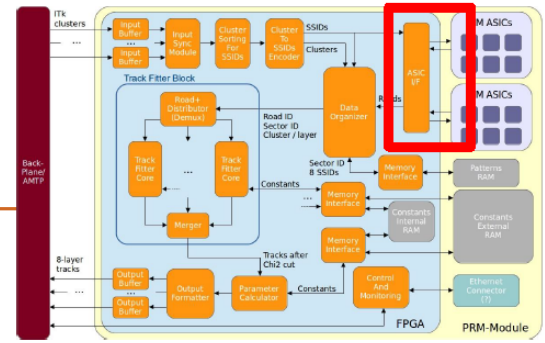
- Which tensions should go from the TP to the Mezzanine?
- Only 12V@xxA, and the others are done by the mezzanine?
- Do we have enough space in the mezzanine to do the other tensions? (if yes, maybe an elegant solution)

Pin-out

- Review what is proposed, and check if it is appropriate/optimal
- Possible proposals: 2 FMC 16 lines TP-to-Mezzanine and 16 lines Mezzanine-to-TP
- Assuming 8Gb/s (32 bits per cluster?) or 12 Gb/s (48 bits per clusters?)

FPGA – AMchip (blue)

The SSIDs are sent to the two groups of AM chips with a maximum frequency of 250MHz. Therefore the maximum speed is 8 layers x 250MHz x 16bits per SSID x 2 groups of AM chips = 64 Gb/s for L1 Track. From the AM chips the PRM receives the RoadID and the 8 layer hitmap.



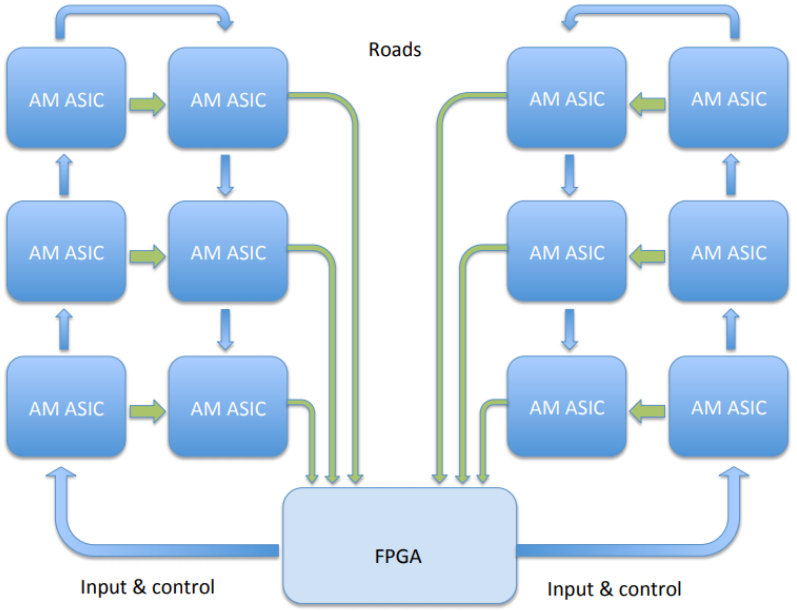
AM ASIC I/F - Data Flow

Interface between the FPGA and the two groups of AM chips

Block Name	Rate at Input (Required)	Input Format	Input Data	Output Format	Output Data	Output Time
AM ASIC I/F	64Gb/s - 250 MHz per AM ASIC group	8 x 16 bit	8 x SSID	23 bits + 8 bits	RoadID + 8 layer hitmap	

- **Data Flow requirements**
  - 8 layers x 250 MHz x 16 bits x 2 groups of AM ASICs = 64 Gb/s

FPGA – AMchip lines



LVDS FPGA-to-AM:

- A possible option: two bus, one for half of the AM chips, one for the other half.
- 33 lines for data +1 line for clock (LVDS 500MHz DDR)
- Synchronisation - skew: probably we should guarantee 200-300 ps

LVDS AM-to-FPGA:

- A possible option: 500MHz, a bus per AM chip, or one serving two AM chips, if not enough pins in FPGA
- 8-9 lines per AM Chip

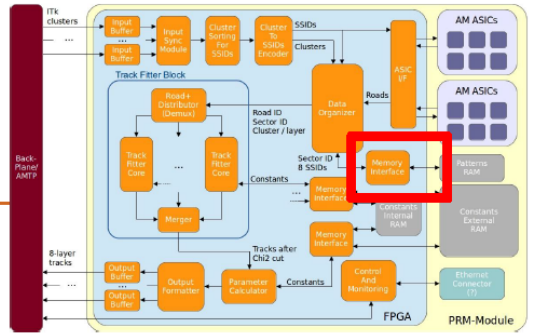
Phase:

Is it possible to control the output phase of the FPGA?

Is it possible to re-adjust the phase in input to the AM chips?

FPGA – RAM (red)

Patterns RAM I/F - Data Flow



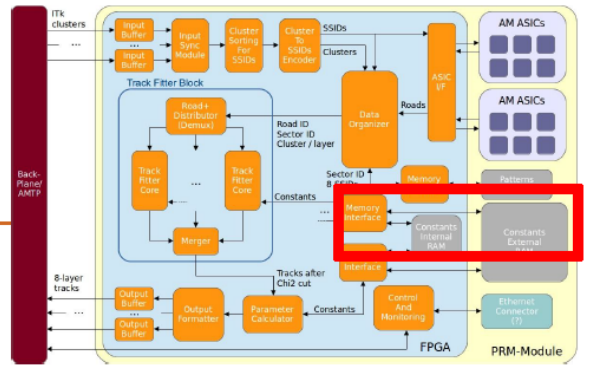
Interface between the FPGA and the Pattern RAM external memory chip

Block Name	Rate at Input (Required)	Input Format	Input Data	Output Format	Output Data	Output Time
Pattern RAM I/F	200 MHz	23 bits	RoadID	16 bits + 8 x 18 bits	SectorID + 8 extSSIDs	

- **Data Flow requirements (Output)**
  - 200 MHz x ((8 x 18) bits (8 extSSID) + 16 bits SectorID) = 32 Gb/s
  - X2 = 64Gb/s for L1 processing
  - 32 Gb/s compatible with 86Gb/s from baseline RAM chip
- **Data Format**
  - RoadID: 23 bits
  - SectorID: 16 bits
  - SSID: 16 bits

FPGA – RAM (red)

Constants External RAM I/F - Data Flow



Interface between the FPGA and the Constants RAM external memory chip

Block Name	Rate at Input (Required)	Input Format	Input Data	Output Format	Output Data	Output Time
Constants External RAM I/F	(30 - 100 MHz) x size	16 bits	SectorID	32 (?) floating point TBD	Constants	

- **Data Flow requirements**
  - 30 MHz from TDR table 13.21, would like to design for 100 MHz (need higher bandwidth from memory)
  - Output BW to be defined after definition of constant size

FPGA – RAM (red)

Two external RAMs are needed for reading SSIDs for the found roads, and constants for the fit. The baseline external RAM device is a reduced latency RAM chip (RLDRAM3) with a 1 Gbit size. The two external RAMs will use approximately 170 FPGA pins. Two seperate intefaces will be designed, one for each external RAM.

The Pattern RAM must store the SSIDs of 4.6M patterns times 176 bits, which is just above 800 Mb. The Pattern RAM must be able to process RoadIDs arriving at 200MHz. Each road will include 8 extSSIDs. The extSSIDs (extended SSIDs) include the 2 DC bits. The data rate at the output of the Pattern RAM will be 200MHz x ((8x18)bits (for the extSSIDs) + 16 bits (for the Sector ID))=32Gb/s.

The size of the fit constants is assumed to be 6k bits, half of which are needed for the chi2 calculation (for the Track Fitter) and half for the calculation of the helix parameters (for the Parameter Calculator). With the proposed device 160k sets of track fitter constants can be stored. The 3k bits required for the chi2 calculation need to be accessed at high rate. The maximum rate allowed is 30 MHz, which is a good match to our requirements.

DC/DC converters

- Estimated needs: 160 A@1V
- If we stay with the design from FTK-LAMB (80W), we need 2 of them, for a total occupancy of 4cmX8cm
- A possible size for the Mezzanine could be 15cmX15cm, so the DC/DC converted could occupy ~15% of the total surface.
- Can this be optimised? better solutions? Need to review all the numbers and estimates.
- Cooling for DC/DC converters: the need cooling, and the could block the air flux - need to identify the proper position
- + 3(?) DC/DC 50W converters

References

- Paolo’s HW presentation
- Calliope’s FW presentation
- PRM specification document
- HTT twiki
- Phase II TDAQ TDR