KØBENHAVNS UNIVERSITET

Niels Bohr Institute

ATLAS EXPERIMENT

CERN

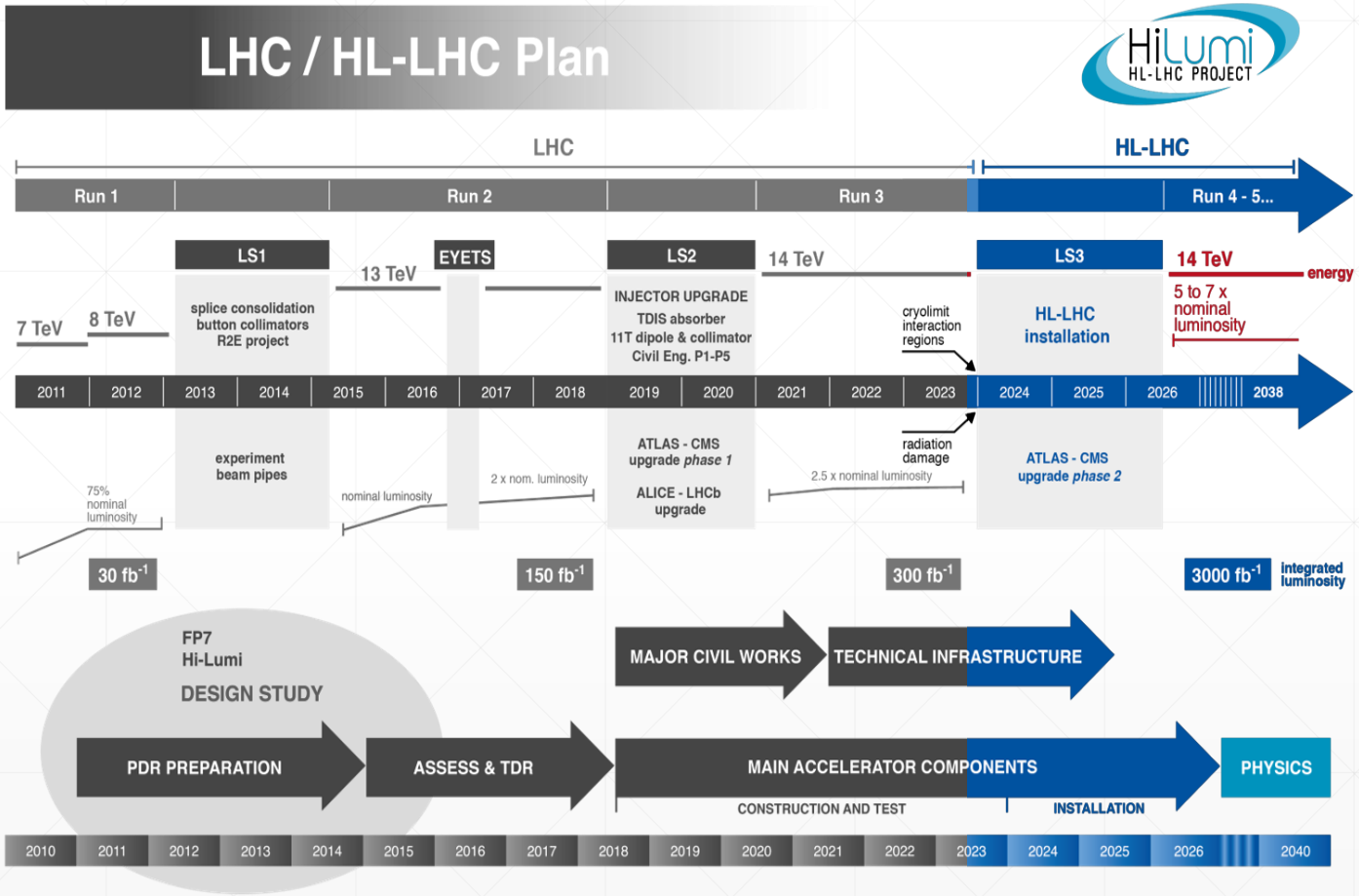
Hardware-based track reconstruction for the ATLAS Trigger and Data Acquisition Phase-II system

Alessandra Camplani – University of Copenhagen

January 5th, 2020

Nordic conference on Particle Physics

LHC and ATLAS plans



Currently, ATLAS is getting ready for the **High-Luminosity LHC** (HL-LHC) [1]

- LHC upgrade will allow to achieve a luminosity value (how many particles are brought to the collision point) **a factor of ten larger than the LHC nominal value**

➢ The ATLAS community is working on the development **of new electronics and detector components:**

- E.g. upgrade of the Trigger and Data Acquisition system (**TDAQ**)

[1] https://cds.cern.ch/record/2284929/files/40-39-PB.pdf

What is TDAQ?

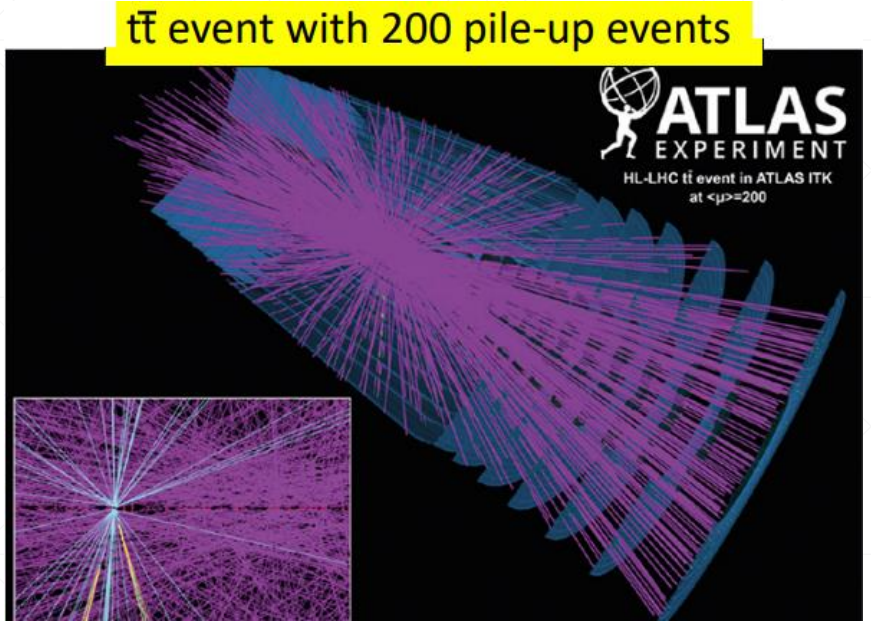
TDAQ system:

- **Selects events** with distinguishing characteristics that make them interesting for physics analyses
  - **reducing** the flow of data to manageable levels
- Passes interesting events on to a **data storage** system for offline analysis

Currently the ATLAS trigger system carries out the selection process in **two stages**:

- **The Level-1 hardware trigger**, constructed with custom-made electronics, works on a subset of information from the calorimeter and muon detectors.
- **The High Level Trigger (HLT)** is a large farm of CPUs (i.e. a software based trigger) which refines the analysis of the hardware-based Level-1 trigger.

Challenges and physics motivation



High luminosity consequences

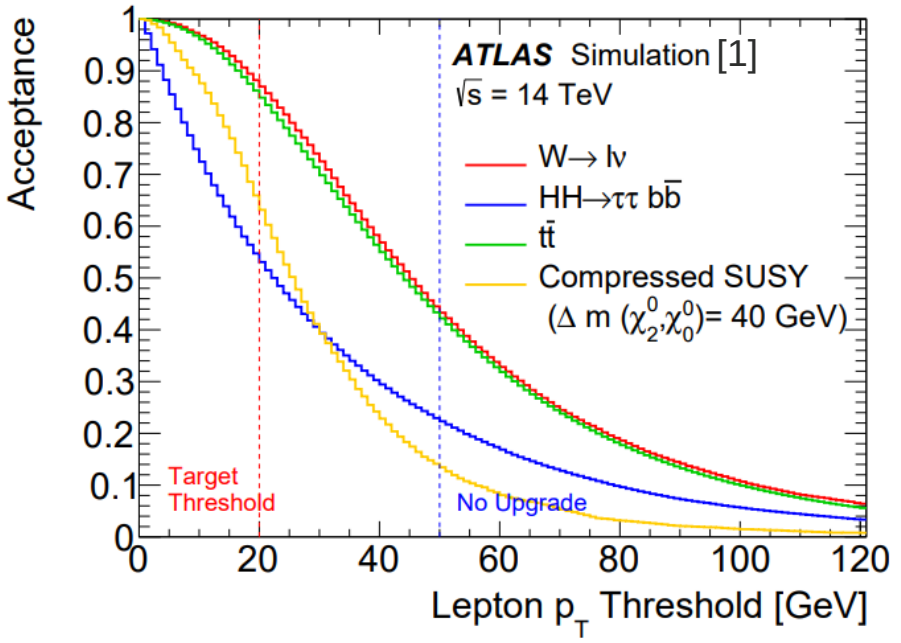
- High pile-up up to 200 events per bunch crossing (<μ>~40 today)
- High granularity detectors that need to be read out
  - new subdetector: Inner Tracker (ITk)
- Larger event size ~5.2 MB (~2 MB today)

The **challenging and broad HL-LHC program** requires the pT of the various trigger objects as low as possible, e.g.:

- Electroweak scale requires low pT leptons
- Searches for new physics with low Δm
- HH measurements requires low pT jets /b-jets

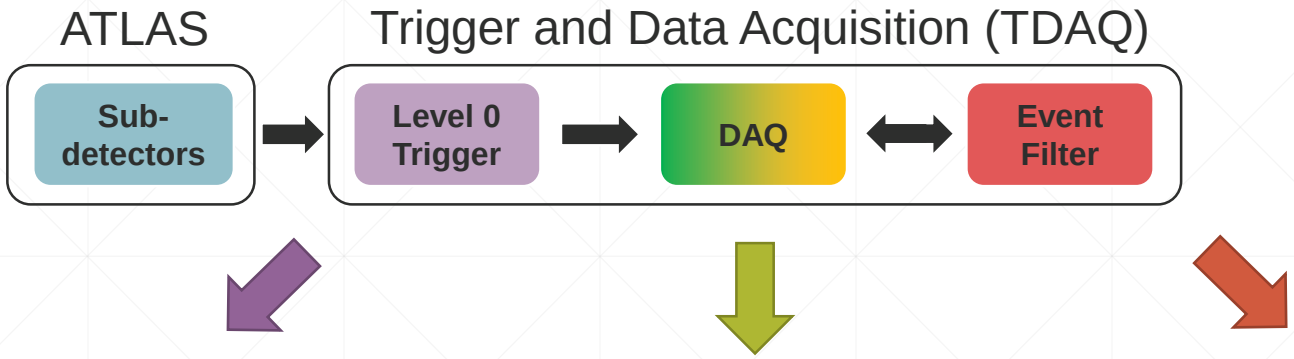
Changes in the operating points for ATLAS TDAQ:

- Level 1 trigger latency increase to ~ 10 μs (~2.5 μs today)
- Readout rate increase to 1-4 MHz (100 kHz today)
- Rate to permanent storage ~ 10 kHz (~1 kHz today)



[1] https://cds.cern.ch/record/2285584/files/ATLAS-TDR-029.pdf

Overview of the Phase II TDAQ systems

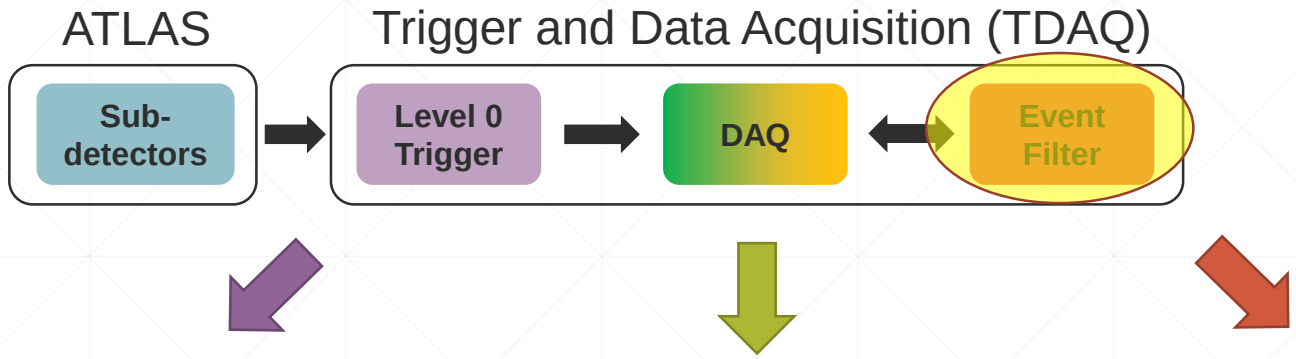


- Data from calorimeters and muons are used for a first selection.
- Identification algorithm, are applied.
- Digital trigger inputs are aligned and combined to make the final Level-0 Accept decision.

- Data from the ATLAS detector front-end electronics are received and formatted.
- Dara are buffered before, during and after the Event Filter decision.
- Finally selected events are transferred to permanent storage.

- Algorithms close to the offline reconstruction methods will run on a processor farm.
- Track reconstruction is performed by a co-processor
- Info are sent back to DAQ.

Overview of the Phase II TDAQ systems

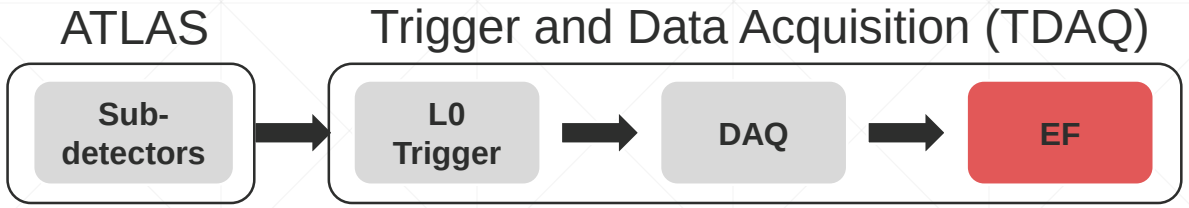


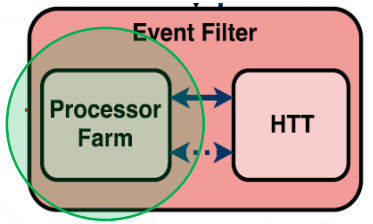
- Data from calorimeters and muons are used for a first selection.
- Identification algorithm, are applied.
- Digital trigger inputs are aligned and combined to make the final Level-0 Accept decision.

- Data from the ATLAS detector front-end electronics are received and formatted.
- Dara are buffered before, during and after the Event Filter decision.
- Finally selected events are transferred to permanent storage.

- Algorithms close to the offline reconstruction methods will run on a processor farm.
- Track reconstruction is performed by a co-processor
- Info are sent back to DAQ.

Event Filter





High pile-up conditions: higher occupancy of tracking detectors and reduced energy resolution in calorimeters

➢ higher trigger rates and/or worse efficiency

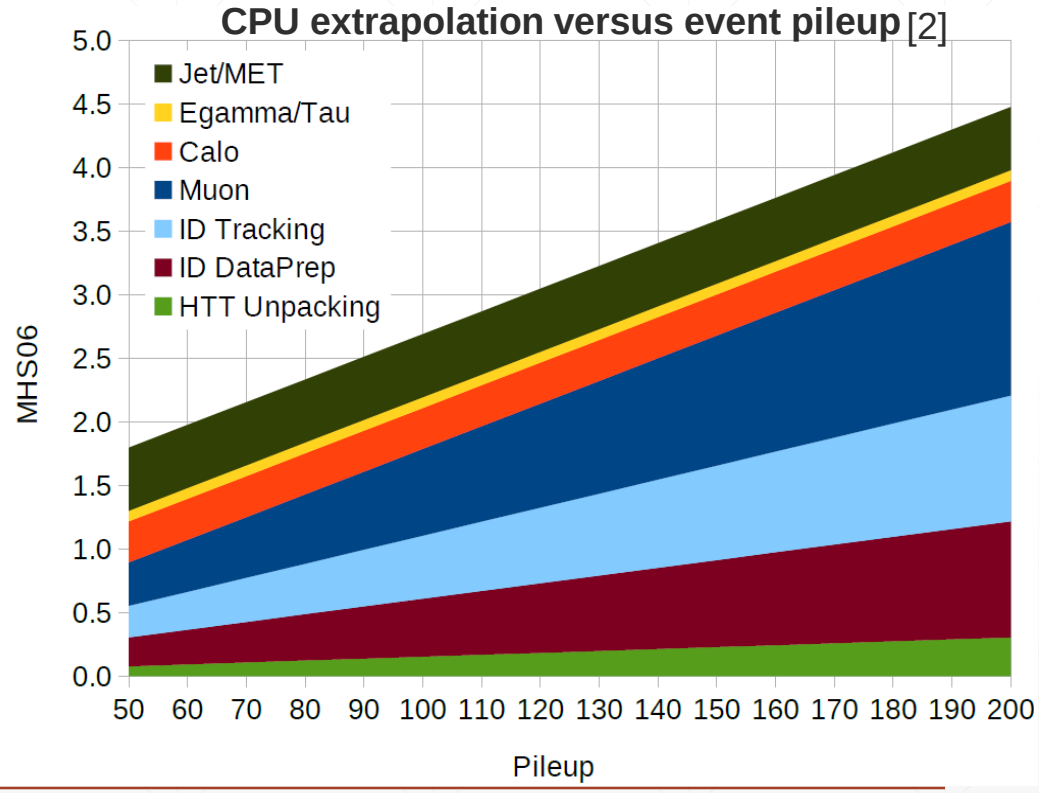
To maintain threshold similar to Run1:

1. algorithms close to the offline reconstruction methods
2. tracking to identify a primary vertex and associate reconstructed objects

1) Processor Farm:

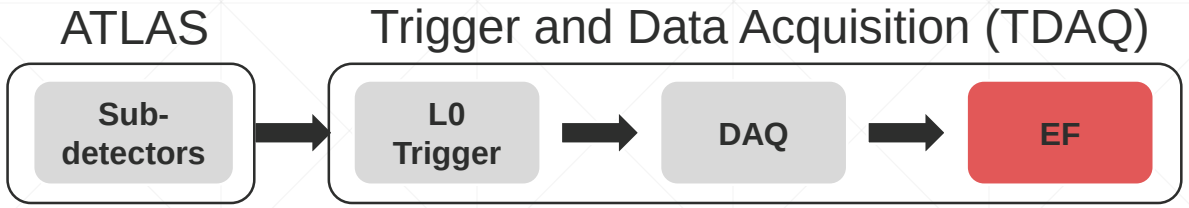
The current baseline assumption is that **CPUs will provide the required compute density** on the time-scale of Phase-II:
Current estimate of farm size:

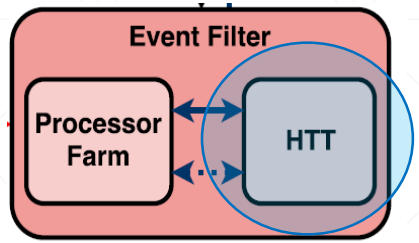
- 4.5 MHS06[1] (+Hardware Track Trigger) to handle a L0 rate of 1 MHz



[1] More about HEP-SPEC06 (HS06) unit can be found at this link
[2] https://cds.cern.ch/record/2285584/files/ATLAS-TDR-029.pdf

HTT system



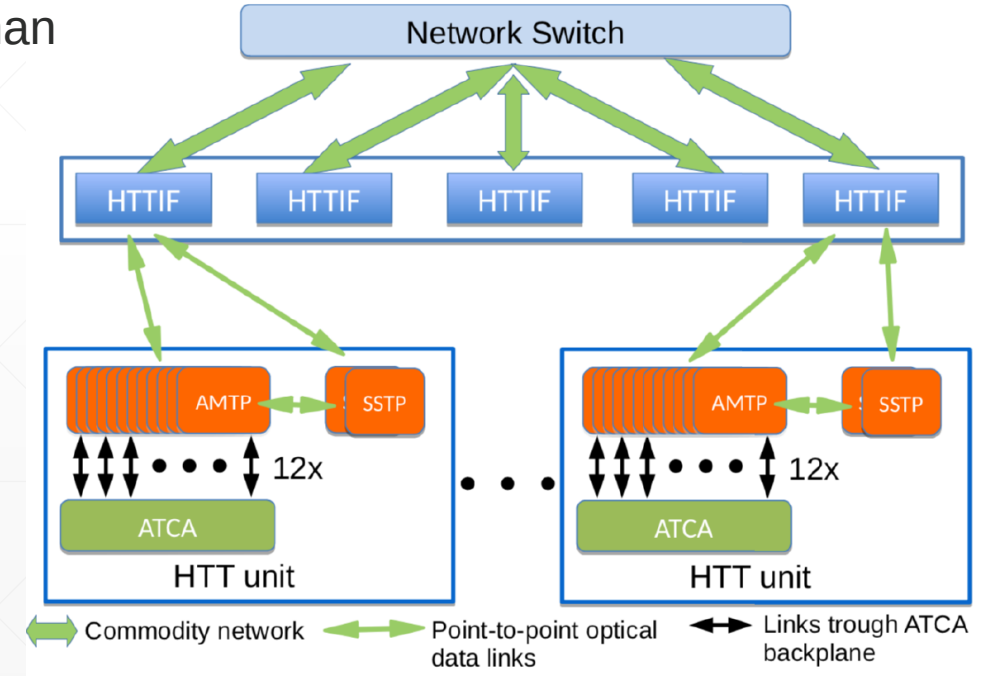


2) Hardware Track Trigger (HTT) co-processor is a new **massively parallel system**, based on Field Programmable Gate Arrays (**FPGAs**) [1,2] and custom Associative Memories (**AM ASICs**) [3].

Goal of the HTT project: perform **very fast reconstruction** (faster than what can be done in software) of particle tracks.

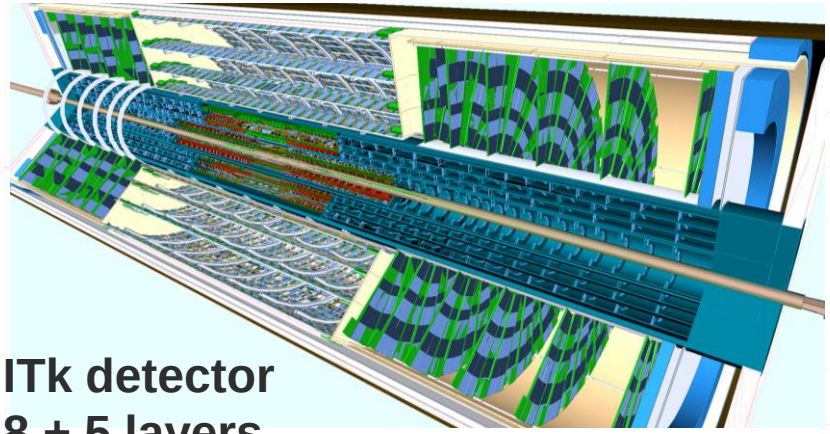
The HTT is organized as an array of independent tracking units called HTT units, each containing:

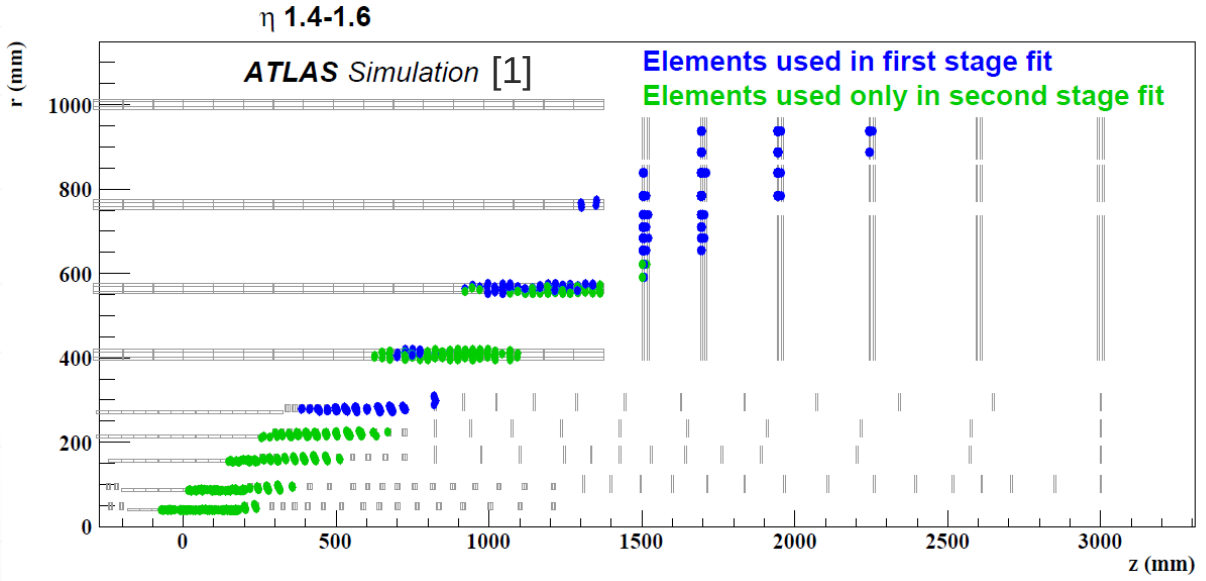
- **Associative Memory Tracking Processors (AMTPs)**:
  - Track reconstruction through pattern recognition on 8 Inner Tracker (ITk) detector layers and track fitting
- **Second Stage Tracking Processors (SSTPs)**
  - 13 ITk layers (all) track extrapolation and fitting



[1] https://www.intel.com/content/www/us/en/products/programmable/fpga/new-to-fpgas/resource-center/overview.html
[2] https://www.xilinx.com/products/silicon-devices/fpga/what-is-an-fpga.html
[3] https://cds.cern.ch/record/2320701/files/CERN-OPEN-2018-003.pdf

Tracks reconstruction





From Itk detector: hit position, per each layer.

Track reconstruction: performed with either 8 or 13 ITk layers.

[1] https://cds.cern.ch/record/2285584/files/ATLAS-TDR-029.pdf

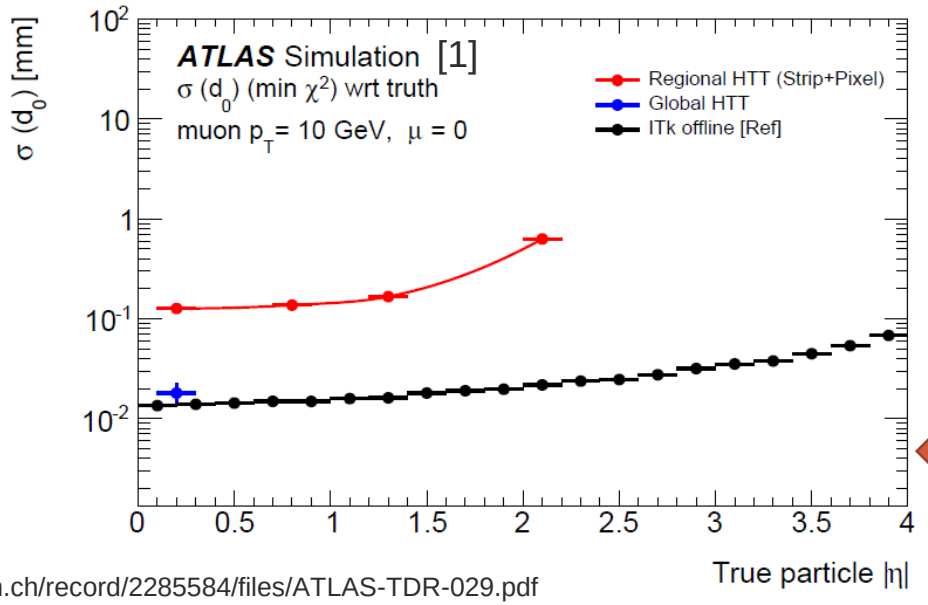
Two-step tracking in HTT

Regional HTT (rHTT)

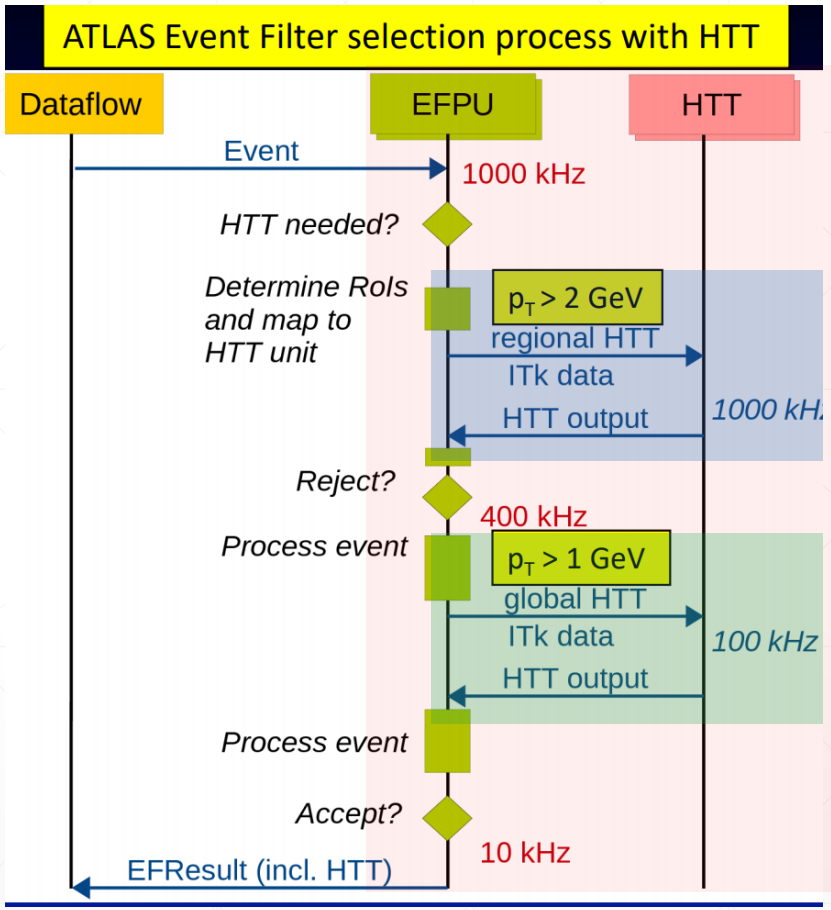
- **Event** from DAQ to EF Processing Units (EFPU)
- **Partial tracker event** data (8 outermost layers) from EFPU to HTT (pT > 2 GeV)
- EFPU uses **rHTT tracks** in combination with Level 0 Trigger information to reduce the rate to **400 kHz**

Global HTT (gHTT)

- If required, **full hit data** (strip and pixel) from EFPU to HTT
- **Full tracking** (pT > 1 GeV) performed
- **EFPU uses gHTT tracks**, in combination with offline-like analysis, to the reduce the rate to **10 kHz**



d0 resolution for 10 GeV muons as a function of η for the HTT first and second stage processing and offline tracking resolution.



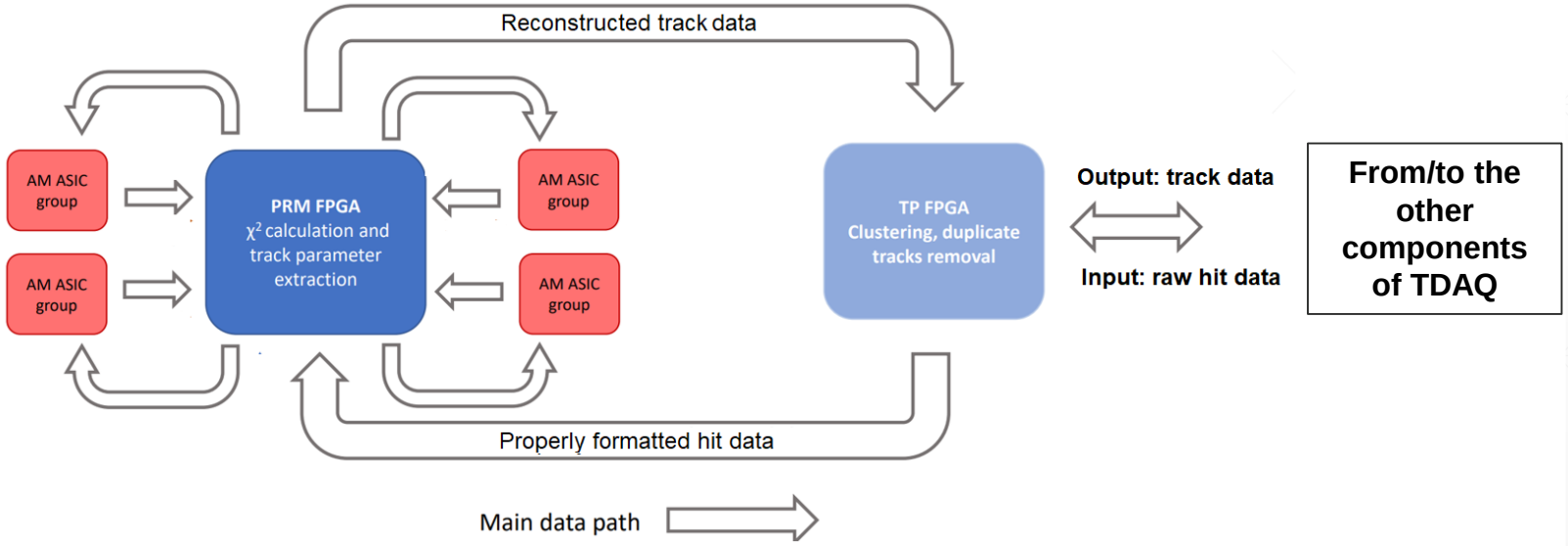
[1] https://cds.cern.ch/record/2285584/files/ATLAS-TDR-029.pdf

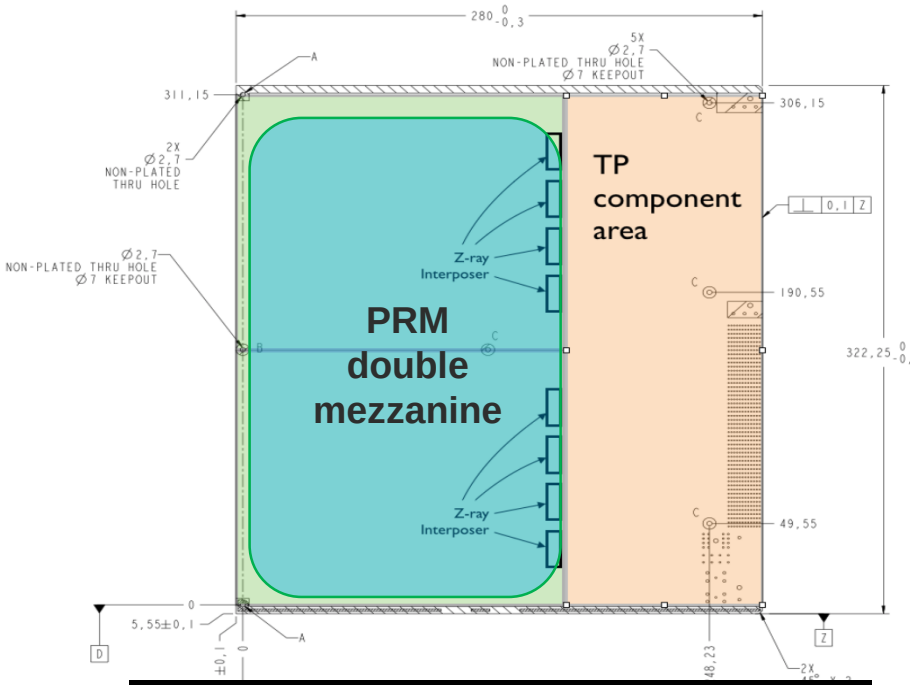
AMTP and PRM

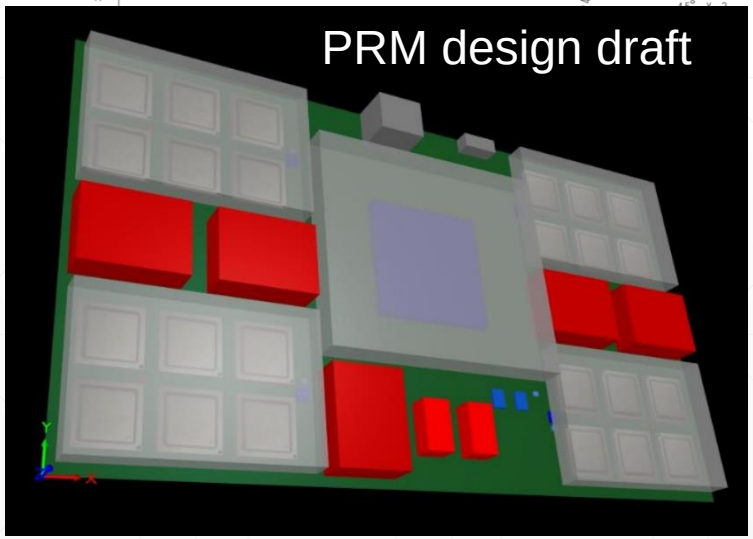
Associative Memory Tracking Processors (**AMTP**) is used for **both regional and global HTT tracking.**

- Carrier board called Tracking Processor (TP)
- Mezzanine called Pattern Recognition Mezzanine (PRM)

Both mounting state-of-the-art **FPGAs**, PRM also has dedicated **custom AM ASICs**.

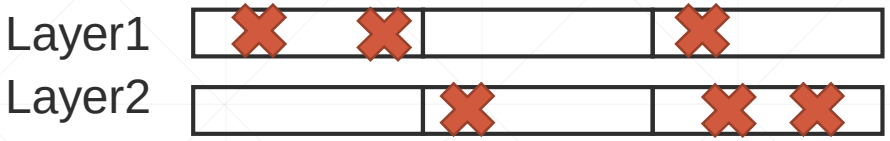


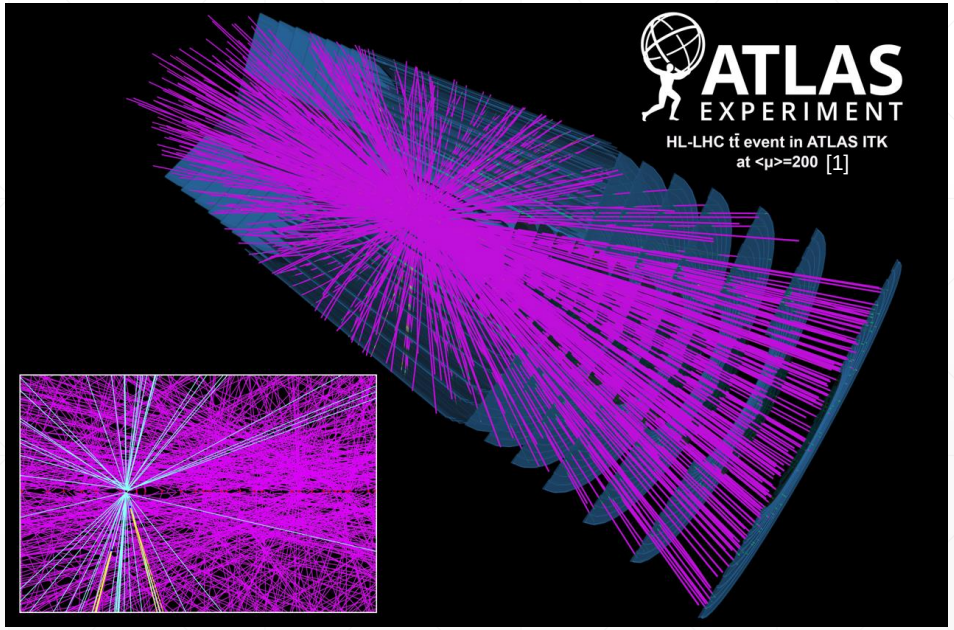




PRM functionality

PRM is doing the first track selection and reconstruction in HTT!



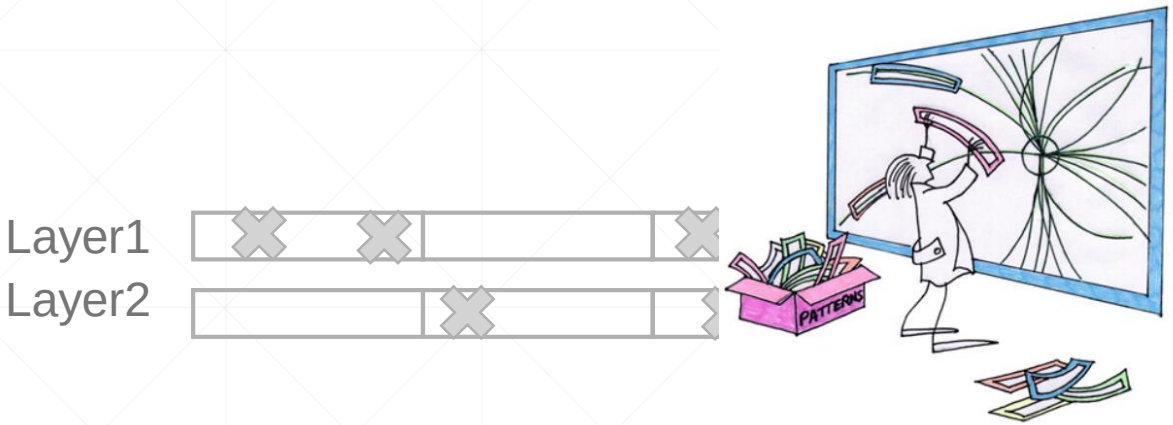


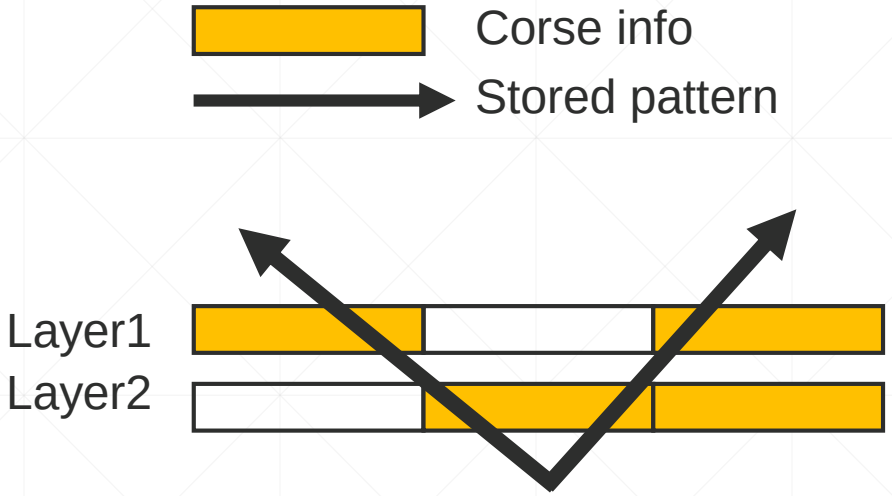
What is sent to PRM:
Charge particle hits info, from 8 layers of the Inner Tracker detector

Hit from a charge particle on the detector

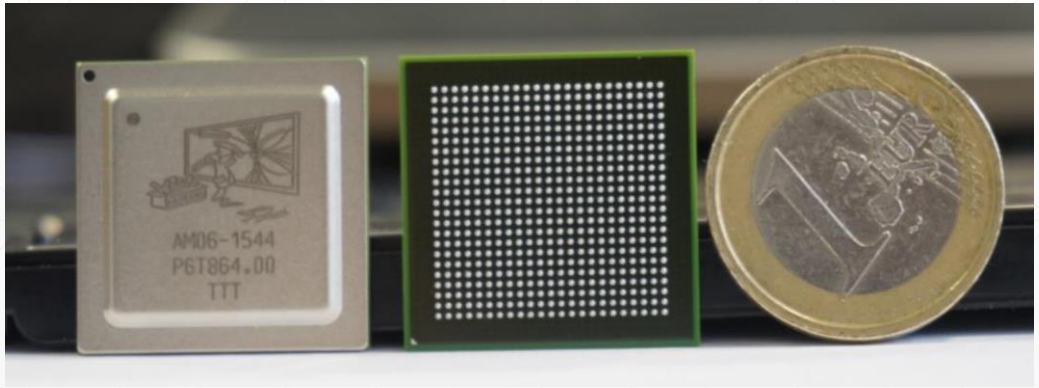
[1] https://atlas.cern/updates/atlas-news/scientific-potential-high-luminosity-lhc

PRM functionality





One custom AM ASIC version 09 will be able to store 384k patterns.



PRM step 1:
Hit information is made coarser (finer info is stored in memories) to allow fast **pattern recognition.**

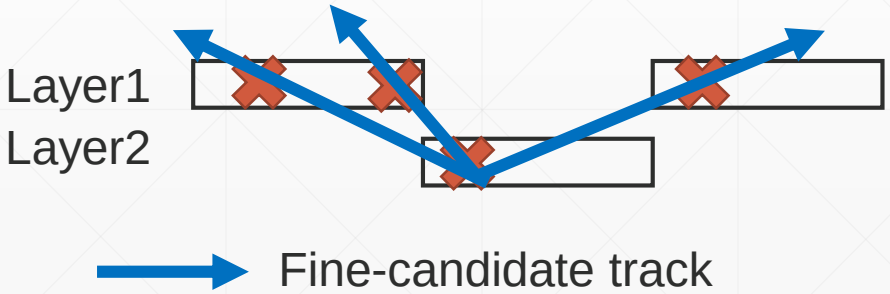
- performed through **AM ASICs** that stores the patterns.

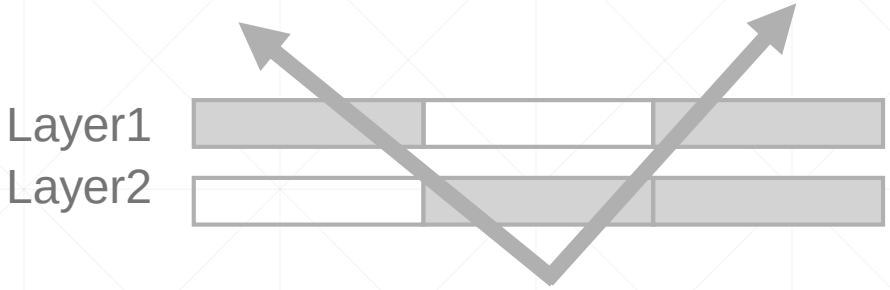
The AM ASICs return coarse-candidate tracks.

PRM functionality

PRM step 2:
Retrieving finer granularity info and building **fine-candidate tracks: can be more than one per each of the coarse candidate track!**

In the FPGA computing χ2 per each candidate and **selecting** the ones with **value lower than a certain treshold.**





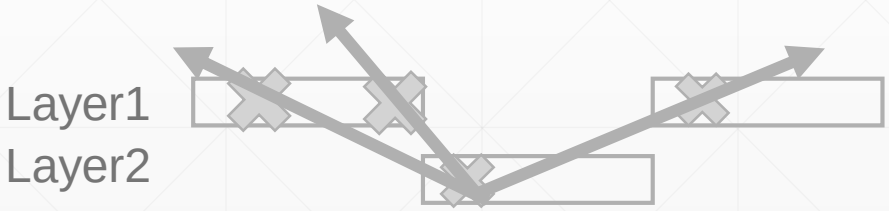
PRM functionality

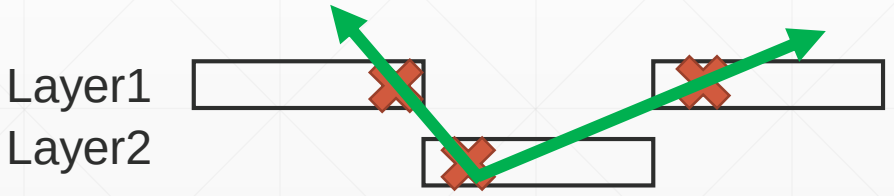
Example of helix parameter ranges used in previous studies [1]

Helix Parameter	Range
d_0	(-32mm, 32mm)
z_0	(-320mm, 320mm)
$\cot\theta$	(-6.55, 6.55)
ϕ_0	$(0, 2\pi)$
Curvature	$(-0.65m^{-1}, 0.65m^{-1})$

PRM step 3 (final):
For the selected track, computing **helix parameter** in the FPGA.

Information is then send back to the TDAQ system to be used for event selection.





Final selected track

[1] http://www.phy.cuhk.edu.hk/sure/comments_2018/whw_rep.pdf

Tracking in trigger menu

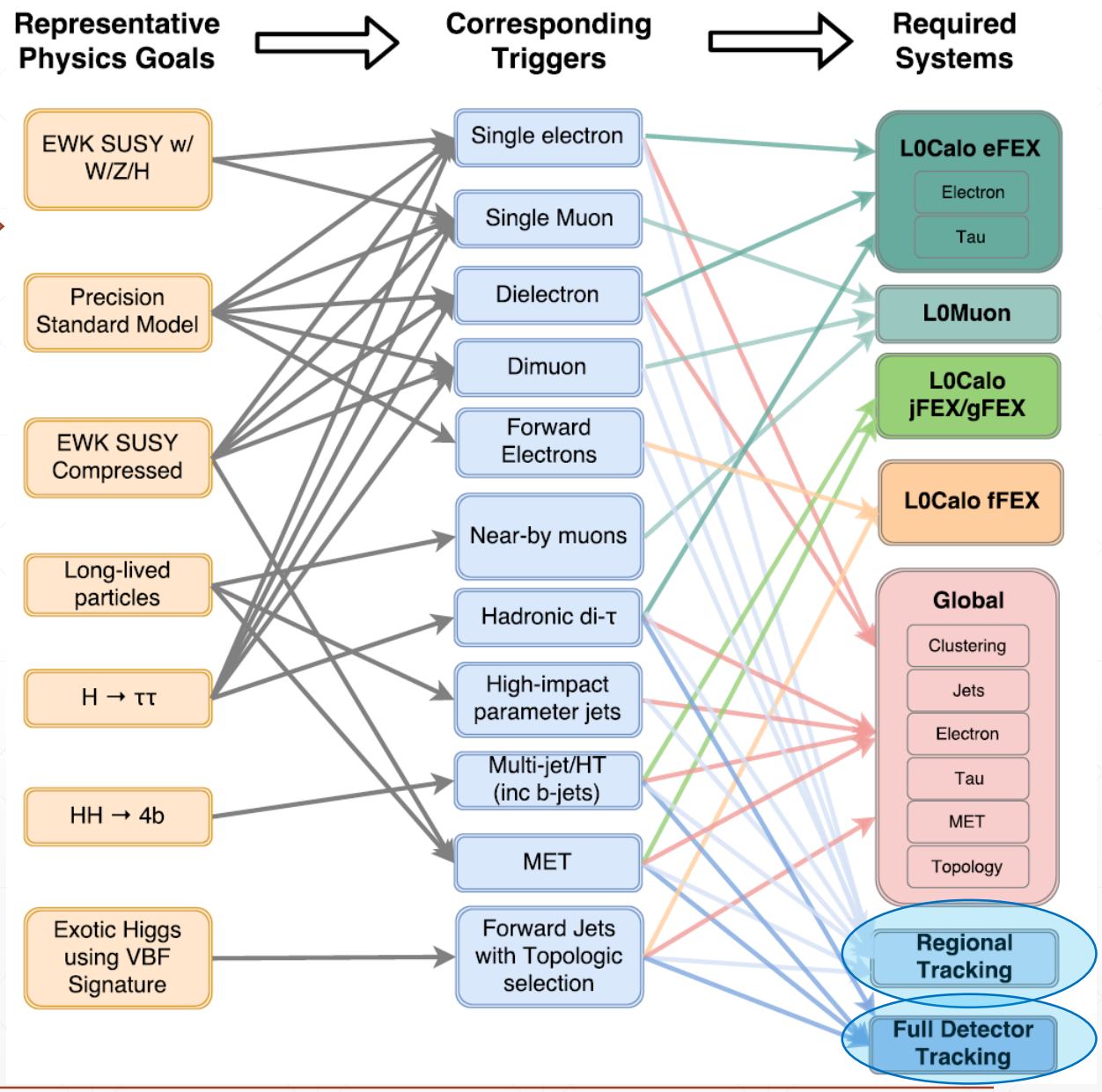
Schematic flow from the representative set of physics goals to the hardware systems needed to achieve them. The middle column lists the **corresponding triggers required.**

E.g.:

1. Global Trigger enables a low-pT electron trigger at Level-0 and then regional-tracking reduces the high rate early in the Event Filter processing.

2. Global Trigger enables low thresholds for multi-jet and Et(miss) triggers at Level-0, then regional tracking and full-detector tracking reduce the background acceptance rate while preserving the physics acceptance.

(Definite plans for the Run 4 trigger menu will come towards the end of Run 3.)



Conclusions

Plans for the ATLAS Trigger and Data Acquisition systems for the High-Luminosity Upgrades are detailed in a Technical Design Report.

The **Hardware Track Trigger** is crucial for the track reconstruction in TDAQ.

The use of **state-of-the-art FPGA and dedicated algorithm** will allow HTT to successfully operate in the challenging scenario foreseen for HL- LHC.

The **Pattern Recognition Mezzanine** is a key element for HTT.

- doing the first track reconstruction and selection in the HTT system

➢ Currently developing **performant hardware and FPGA firmware**
  - necessary to achieve the ATLAS physics goals.

Thanks for your attention!

Backup

Phase-II TDAQ upgrade

Three main systems of the TDAQ Phase-II upgrade architecture:

- Level-0 Trigger
- DAQ (Readout and Dataflow subsystems)
- Event Filter

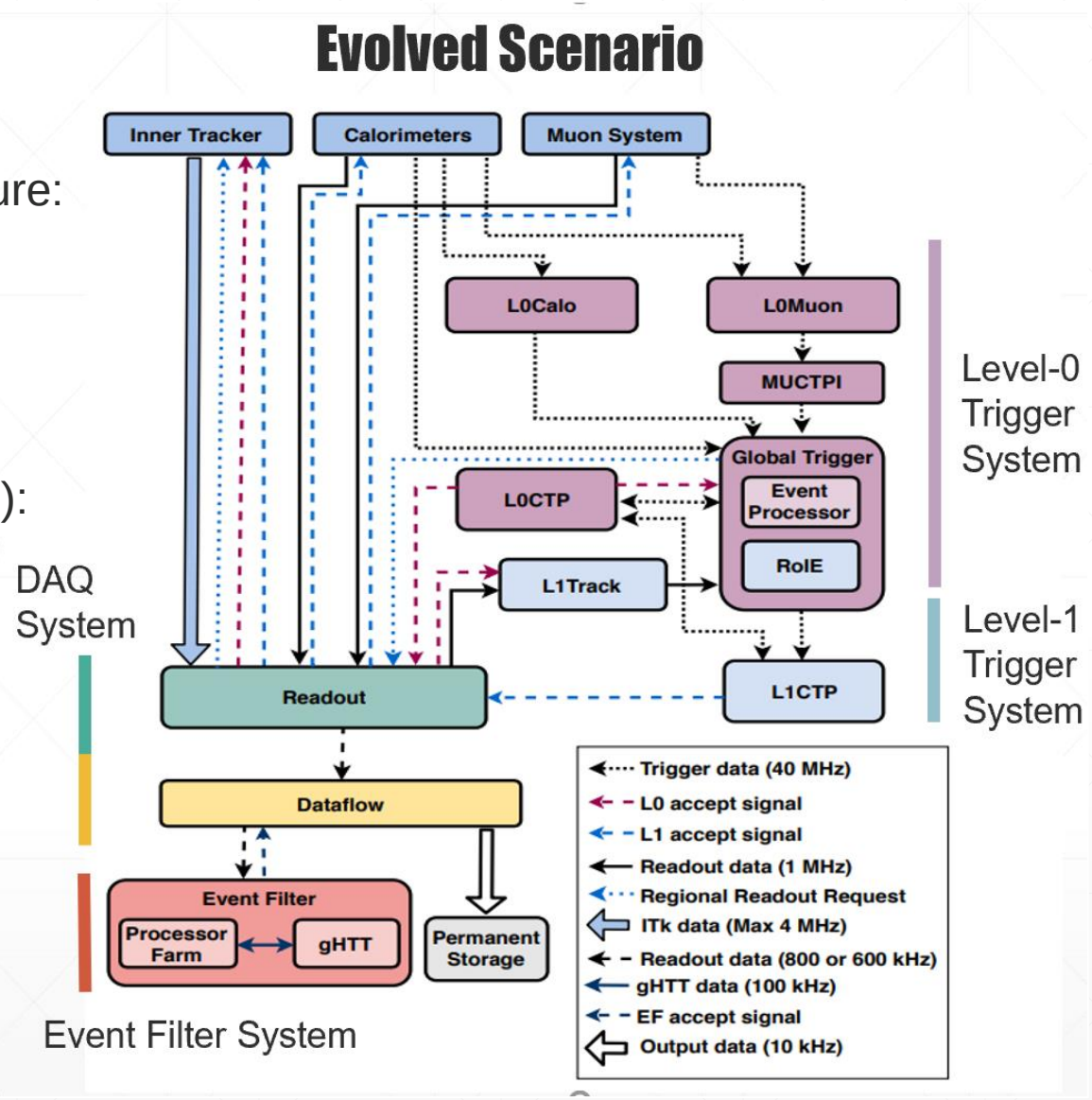
Single-hardware-level trigger architecture (baseline scenario):

➢ capable of evolving into a two-level hardware trigger system (evolved scenario)

The two main **criteria for** an evolution to the **split-level hardware trigger** configuration:

- the hadronic trigger rates
- the inner pixel detector layer occupancies

If either or both are higher than expected, the baseline TDAQ architecture would restrict the trigger menu at the ultimate HL-LHC running conditions.



Reference [1]

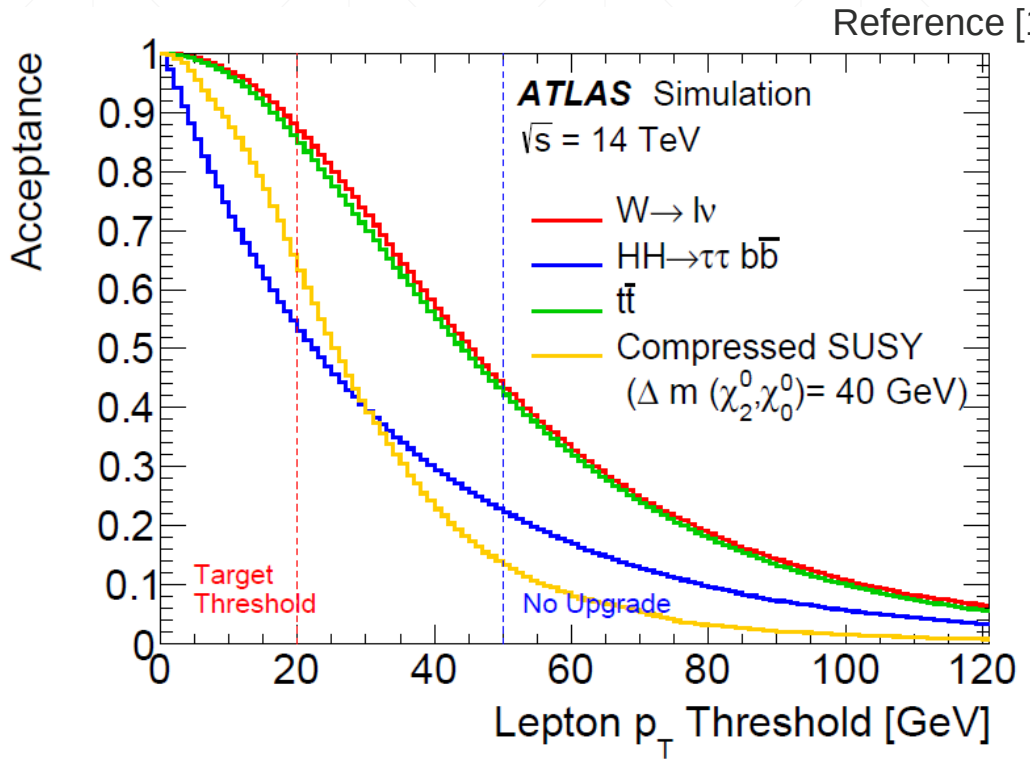
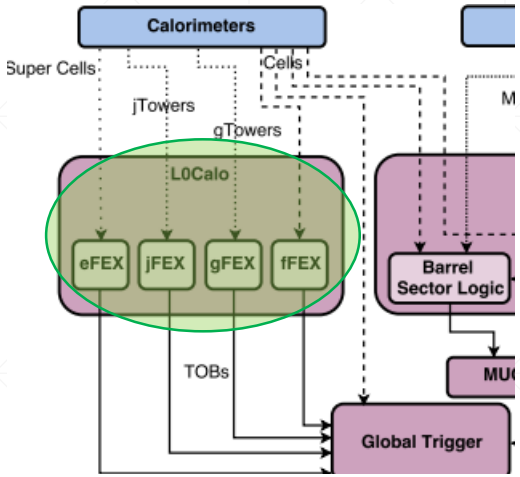


Figure 2.2: *The integrated acceptance as a function of the single lepton p_T threshold for four representative channels: $W \to \ell\nu$, $H \to \tau\tau b\bar{b}$, $t\bar{t}$, and a compressed spectrum SUSY model relevant for "Well-tempered Neutralino" motivated models. The Phase-II TDAQ upgrade would enable lowering the single lepton Level-0 threshold to 20 GeV from 50 GeV, the projected threshold without the upgrade.*

Level-0 Calo



Calorimeters data with coarse granularity are sent to the Feature Extractors (FEXs).

- **eFEX**(1): electron and photon object identification
- **jFEX**(1): single jets identification
- **gFEX**(1): large-R (or multi-jet) triggers identification and global quantities calculation
- **fFEX**(2): forward electromagnetic (forward jet) trigger objects reconstruction at high η

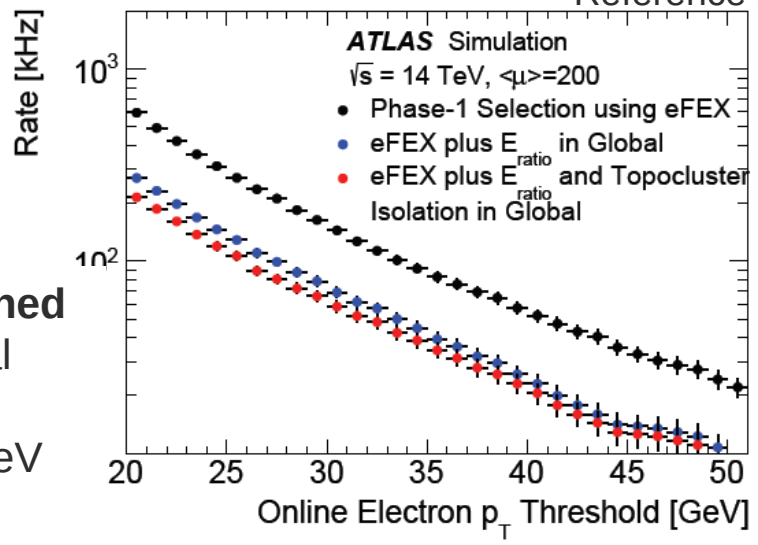
The **Global Trigger refines the identification algorithm** by taking advantage of the transmission of fine-granularity cells

- trigger thresholds can be chosen reasonably low to cover the whole physics program

Subsystem	Trigger Object	Approximate Granularity	Coverage $\lvert\eta\rvert$
eFEX	$e/\gamma, \tau$	Super Cells (10 in 0.1×0.1)	< 2.5
jFEX	τ, jet, E_T^{miss}	0.1×0.1	< 2.5
jFEX	τ, jet, E_T^{miss}	0.2×0.2	$2.5 - 3.2$
jFEX	τ, jet, E_T^{miss}	0.4×0.4	$3.2 - 4.9$
gFEX	Large-R jet, E_T^{miss}	0.2×0.2	< 4.9
fFEX	e/γ	Full detector EMEC, HEC, FCal	$2.5 - 4.9$
fFEX	jet	Full detector FCal	$3.2 - 4.9$

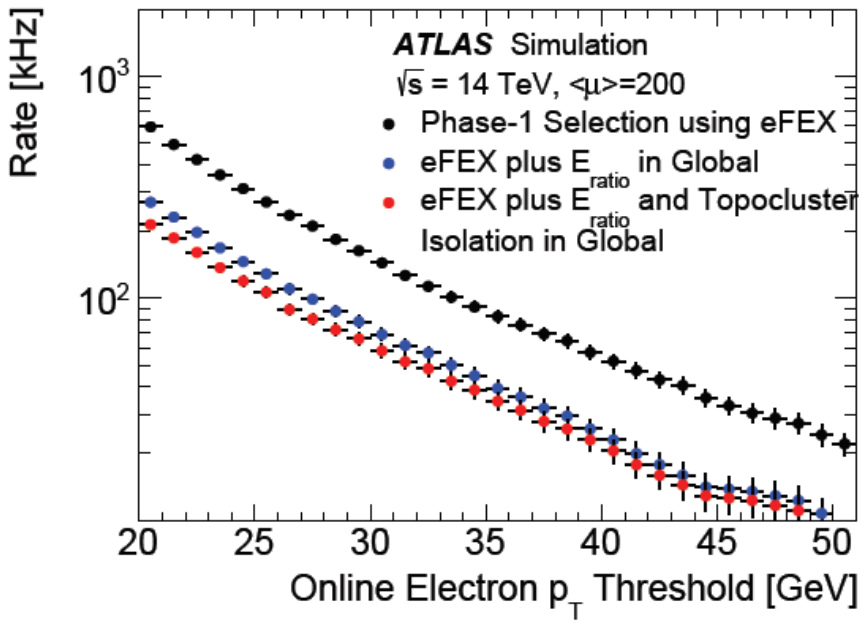
The **performance of the combined system** (Level-0 Calo and Global Trigger) allows to set the single electron threshold at about 20 GeV

Reference [1]

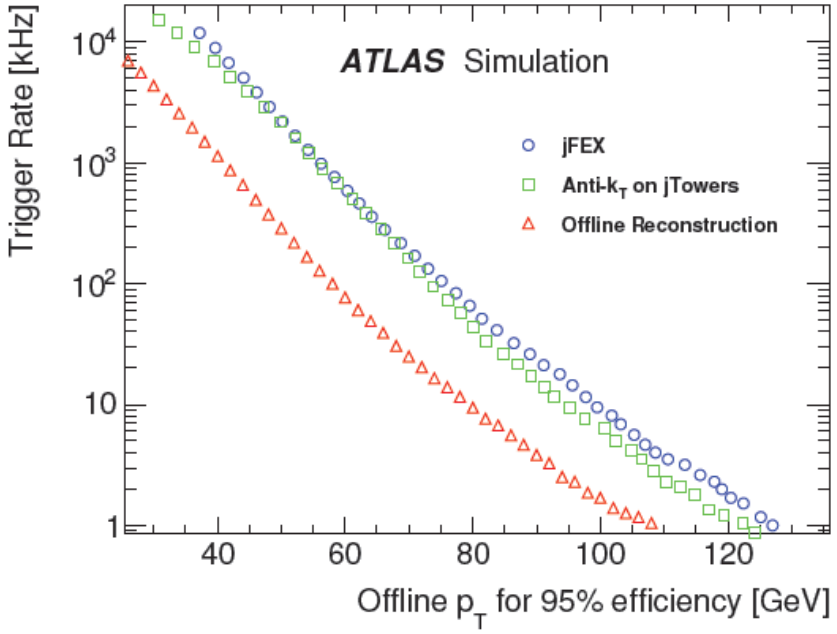


(1) Phase-I Upgrade hardware, firmware upgrade foreseen for Phase-II
(2) New Phase-II system

Reference [1]



(a)



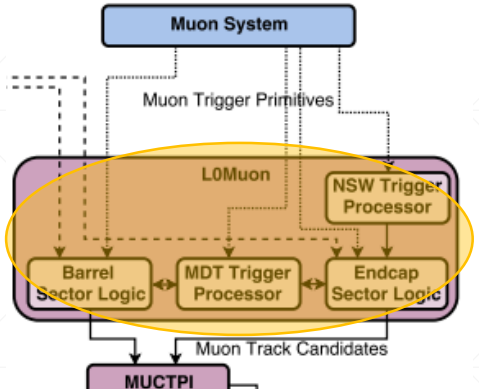
(b)

Figure 7.1: *a) Level-0 trigger rates for electrons. The different curves are for the successive application of veto conditions. b) The forward ($|\eta| > 3.2$) single-jet trigger rate vs. offline p_T thresholds for jets reconstructed in the jFEX. The efficiency is evaluated using $HH \rightarrow bbbb$ signal events, and the trigger rate is evaluated based on minimum bias background events at $\langle\mu\rangle \simeq 200$. The jFEX algorithm, the offline anti-k_t algorithm (run over $\eta \times \phi = 0.1 \times 0.1$ towers), and the full offline reconstruction are compared.*

Level-0 Muon

Based on the data of the upgraded muon spectrometer and the Tile calorimeter

- Improvements in trigger performance will be achieved by increasing
  - detector acceptance
  - momentum resolution (by including new MDT(3) chamber data)



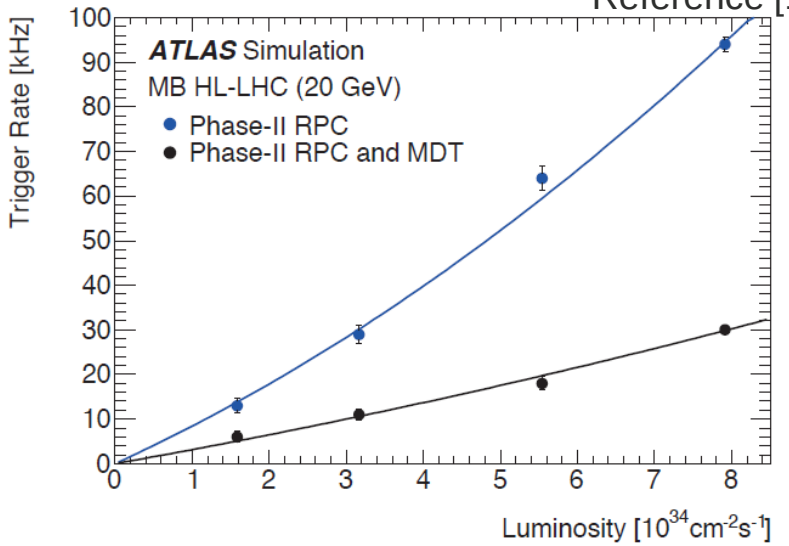
Different detector technologies provide different angular coverage.

Subsystem	Granularity	Coverage $\|\eta\|$
NSW processor (1)	Full NSW detector	$1.3 - 2.4$
MDT processor (2)	Full MDT detector	< 2.4
Barrel Sector Logic (1)	Full RPC and Tile, MDT	< 1.05
Endcap Sector Logic (1)	Full TGC, Tile, RPC, NSW, MDT	$1.05 - 2.4$

Selectivity of the current Level-1 muon trigger is limited by the moderate spatial resolution of RPC (3) and TGC (3).

- MDT chambers will be included in L0 Muon and will provide:
  - better spatial resolution
  - pT resolution close to that of the offline reconstruction

Reference [1]



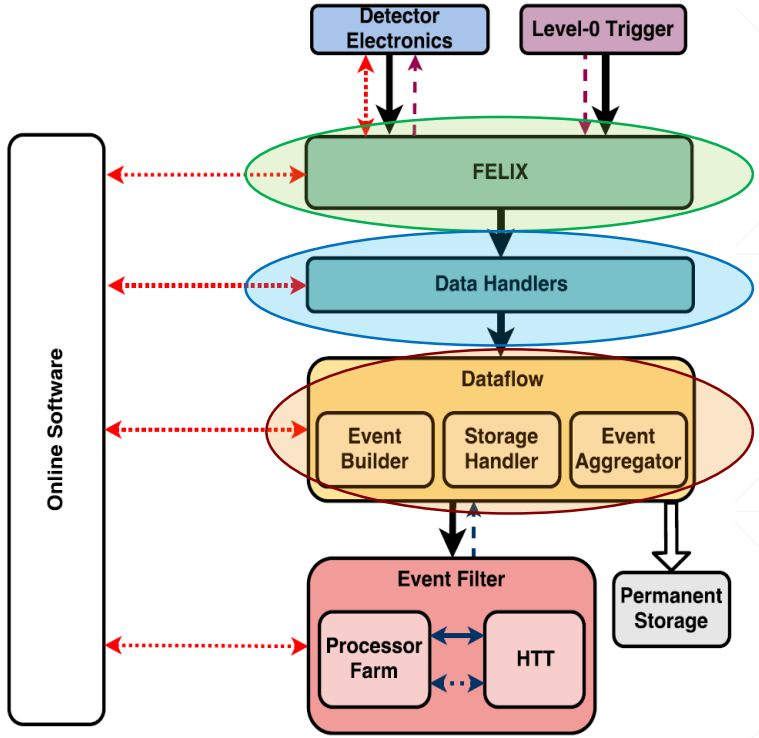
Rate of Level-0 single-muon trigger based on RPC only and RPC plus MDT for the barrel region | η | < 1.05.

(1) Phase-I hardware will be upgraded for Phase-II
(2) New Phase-II system
(3) RPC = Resistive Plate Chambers, TGC = Thin Gap Chambers, NSW = New Small Well, MDT = Monitored Drift Tube

DAQ details

Readout:

- receives data from the ATLAS detector front-end electronics
  - at the L0-trigger rate (1 MHz)
- performs basics processing
- sends them to the Dataflow system



FELIX (Front-End LInk eXchange):

- Custom cards PCIe based
- The new interface to detector-specific electronics including limited detector-specific firmware

Data Handlers:

Servers running a software application that :

- receives event fragments from FELIX
- performs detector-specific formatting and monitoring tasks:

Dataflow:

- Buffers data before, during and after the Event Filter decision
- Provides partial and full event access as needed and transfers data to permanent storage
- Managed by commodity software

Storage Handler

- buffering event data before and during Event Filter processing

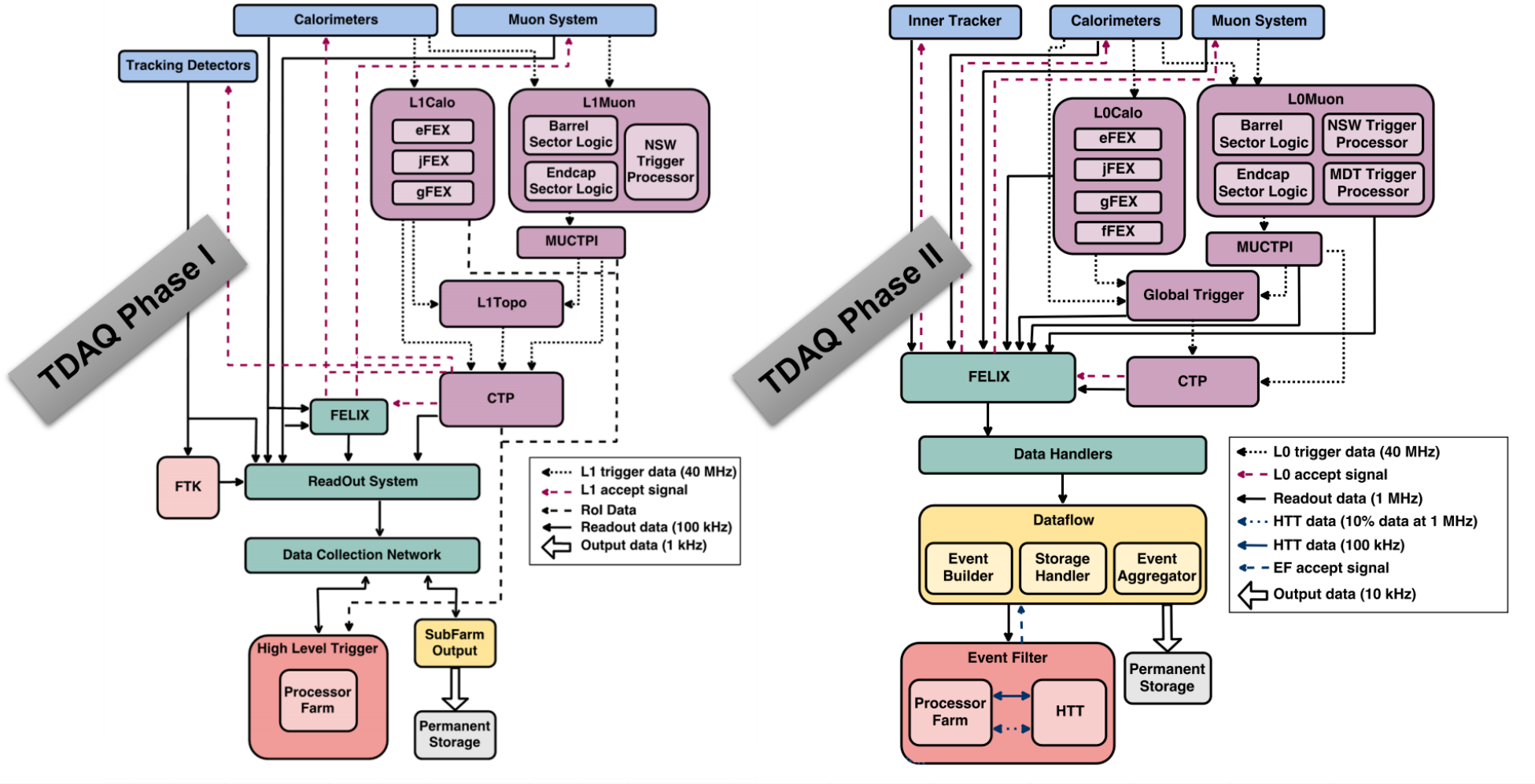
Event Builder

- interface of the dataflow to Data Handlers and Event Filter

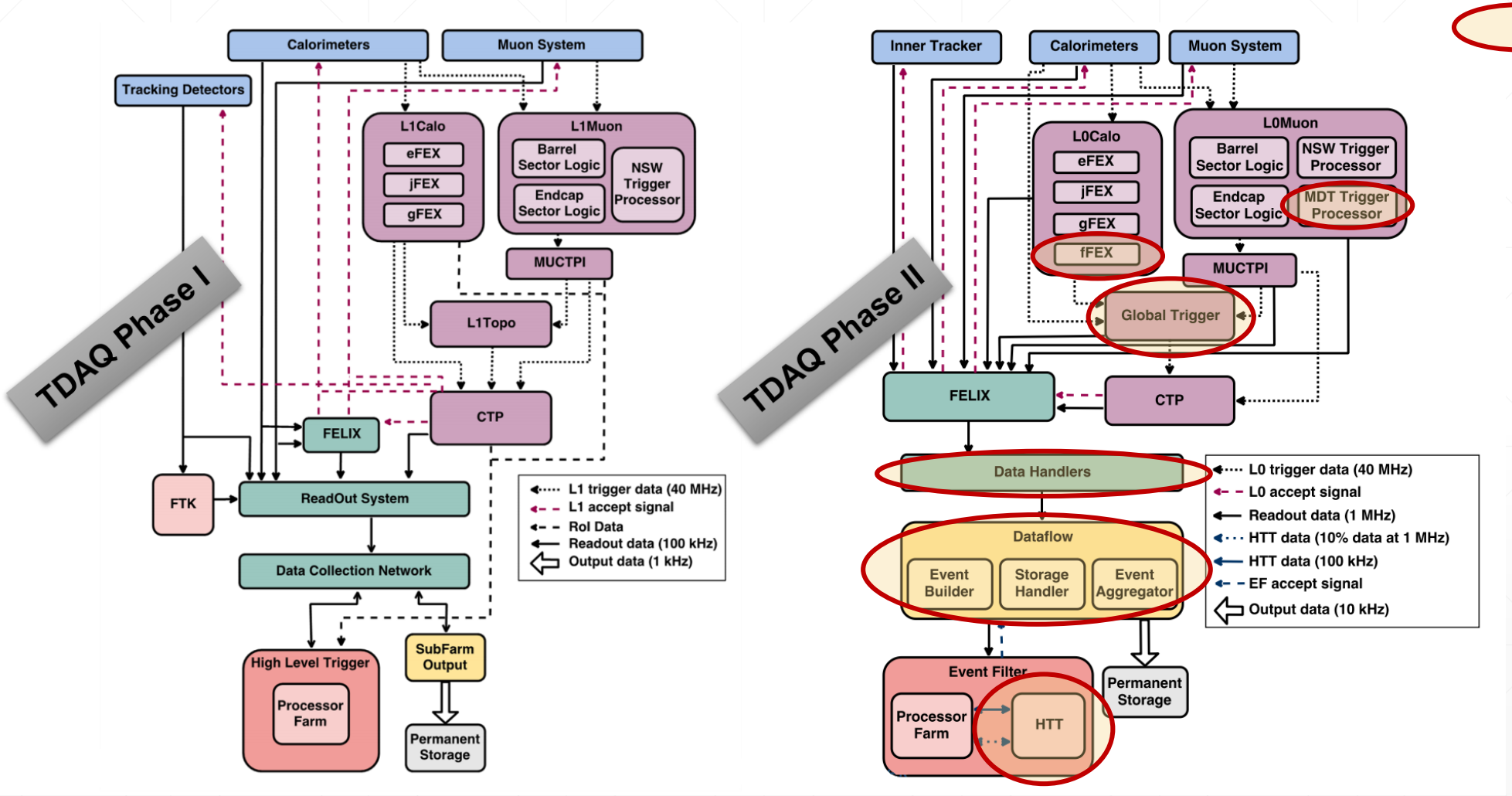
Event Aggregator

- receives the selected events from the Event Filter and groups/compress them before sending them to Tier-0

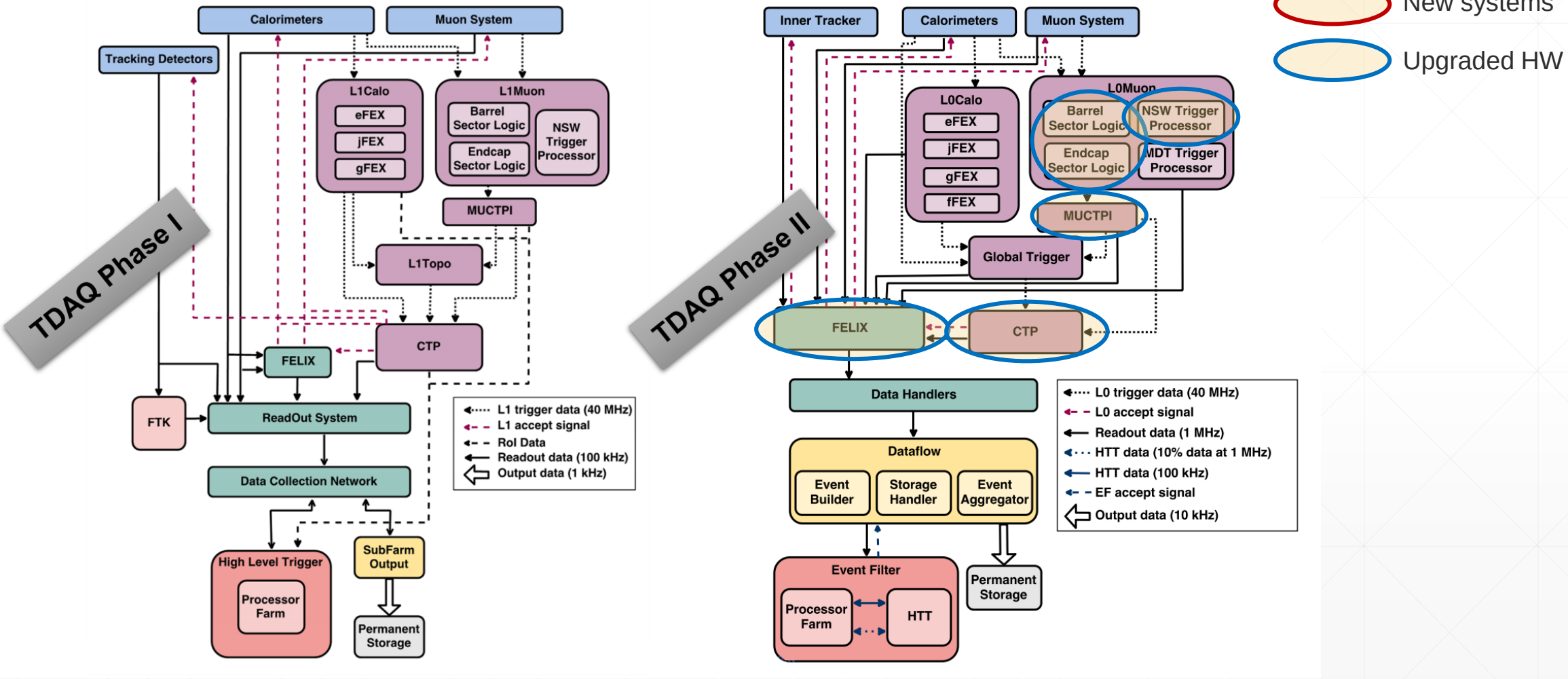
Overview of architecture upgrade



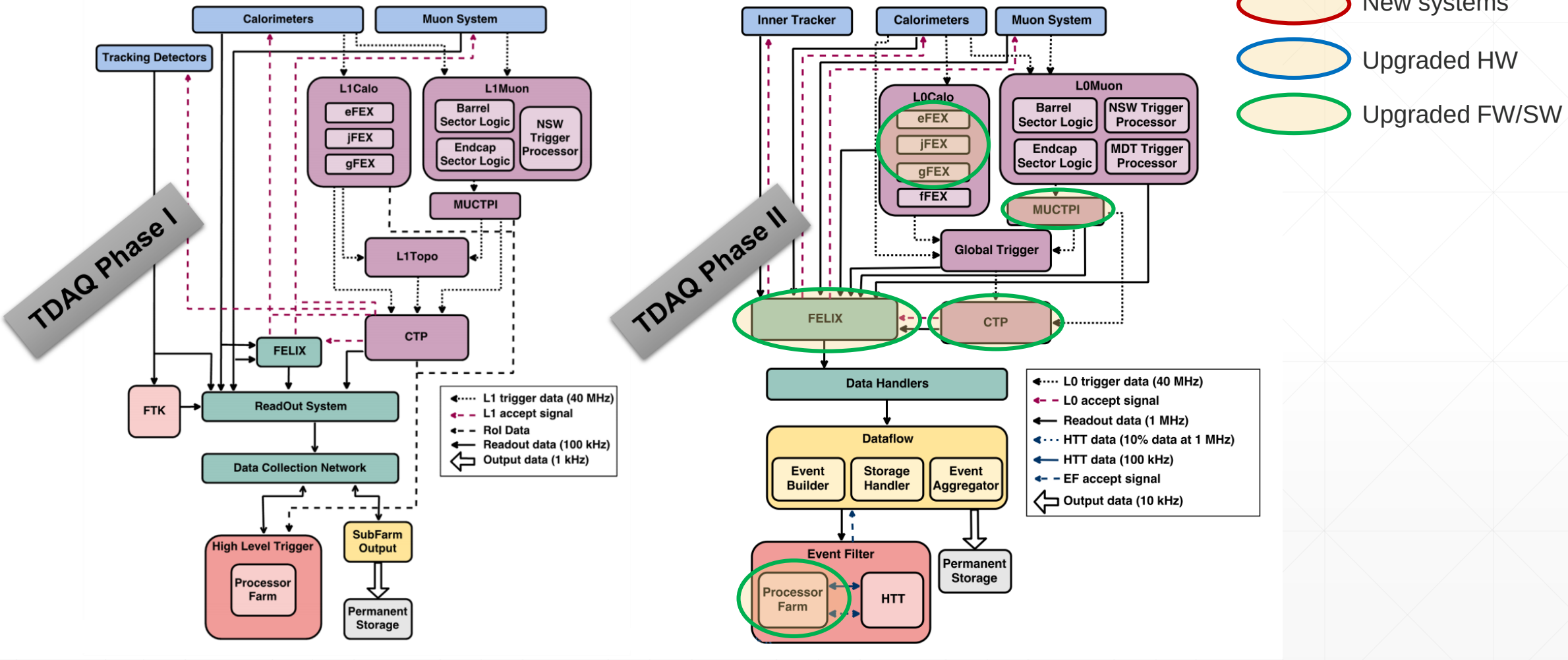
Overview of architecture upgrade



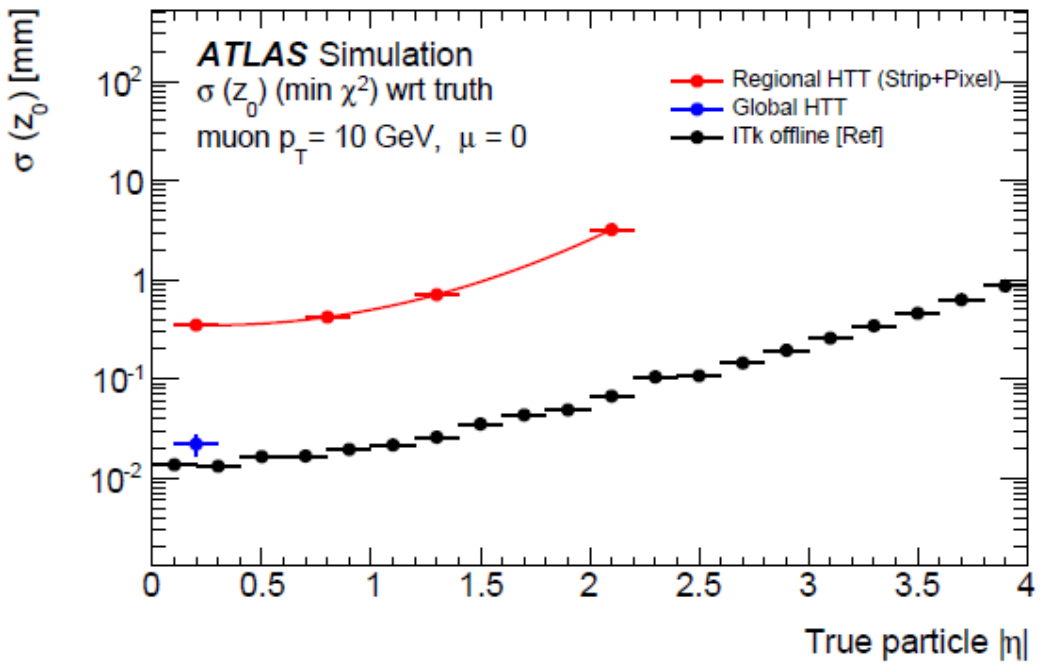
Overview of architecture upgrade



Overview of architecture upgrade



Reference [1]



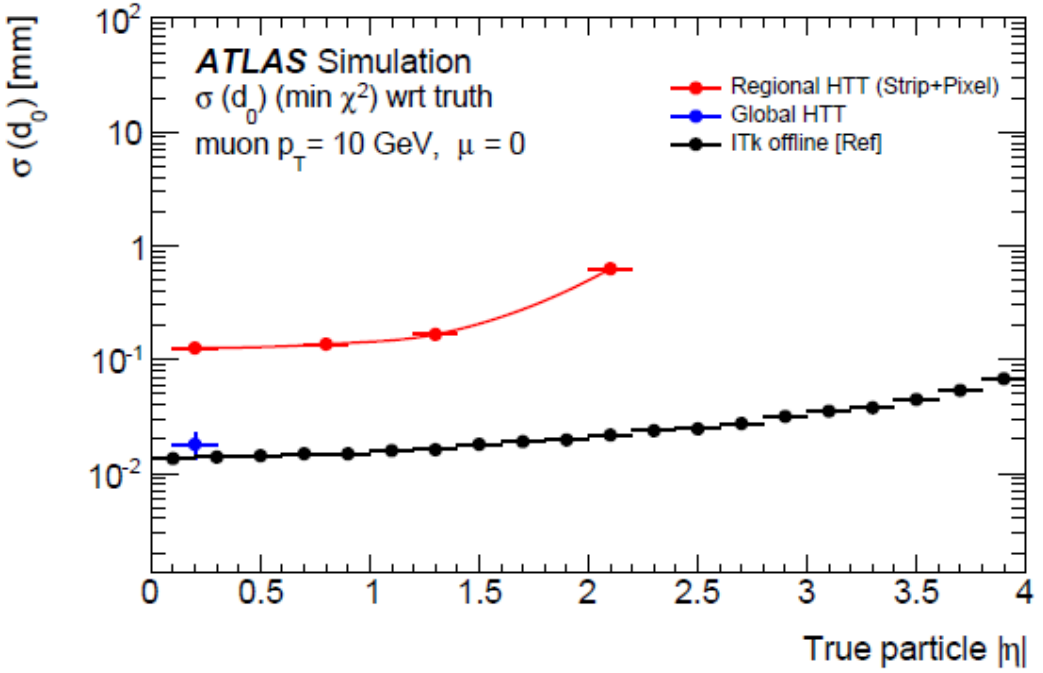


Figure 13.9: *Comparison of the z_0 (left) and d_0 (right) resolution for first- and second-stage fitting and offline.*

What is an Associative Memory

Random-Access Memory (RAM) is a standard type of memory:

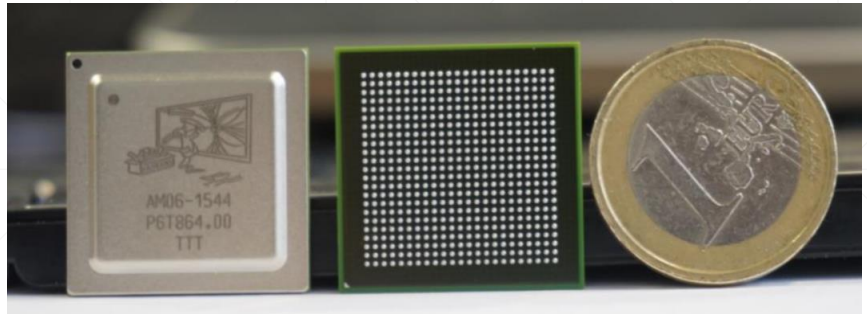
- The search is done by address

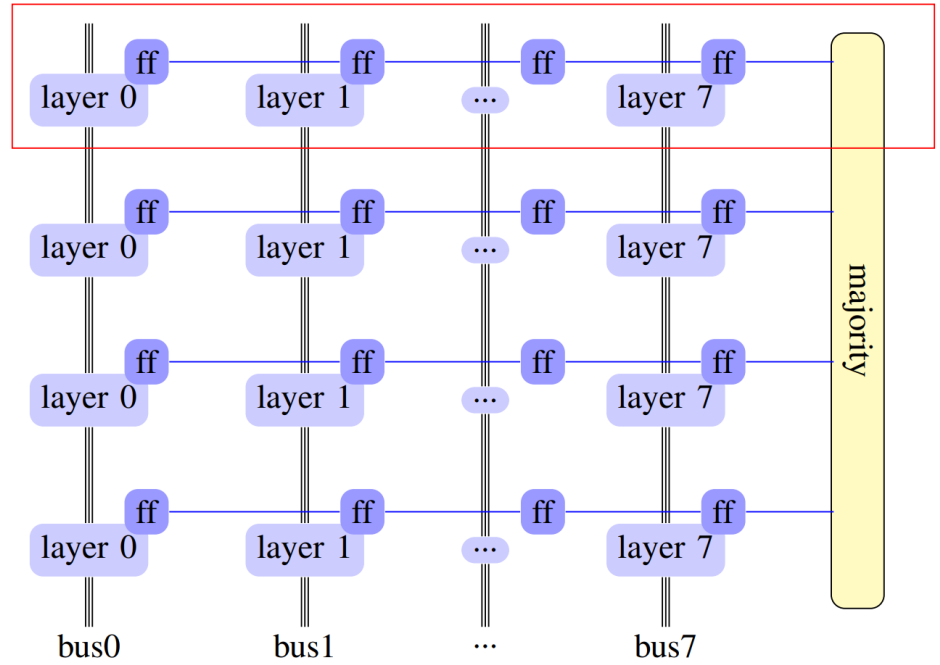
Content-Addressable Memory (CAM) is a special type of memory (also known as associative memory or associative storage):

- The search is done by content

Functionality:

- 8 bus_layers: corresponding to the detector layers
- Cluster information is sent along the bus
- When the content of the AM matches the hit the Flip Flop (FF) is set to 1.
- When more than >= 6 hits are matched along one line, a track is found



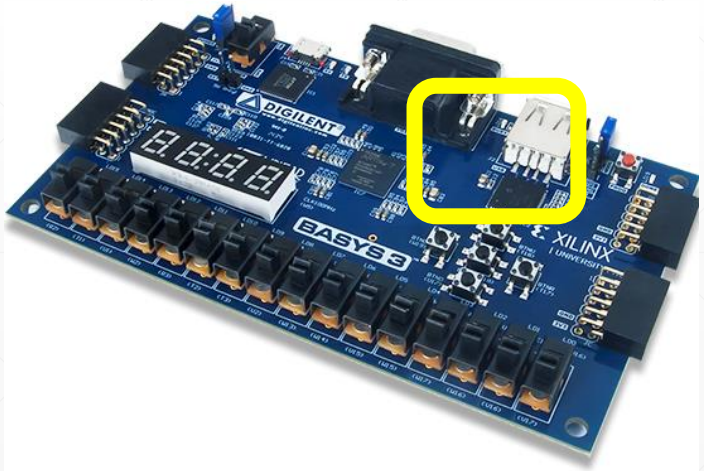


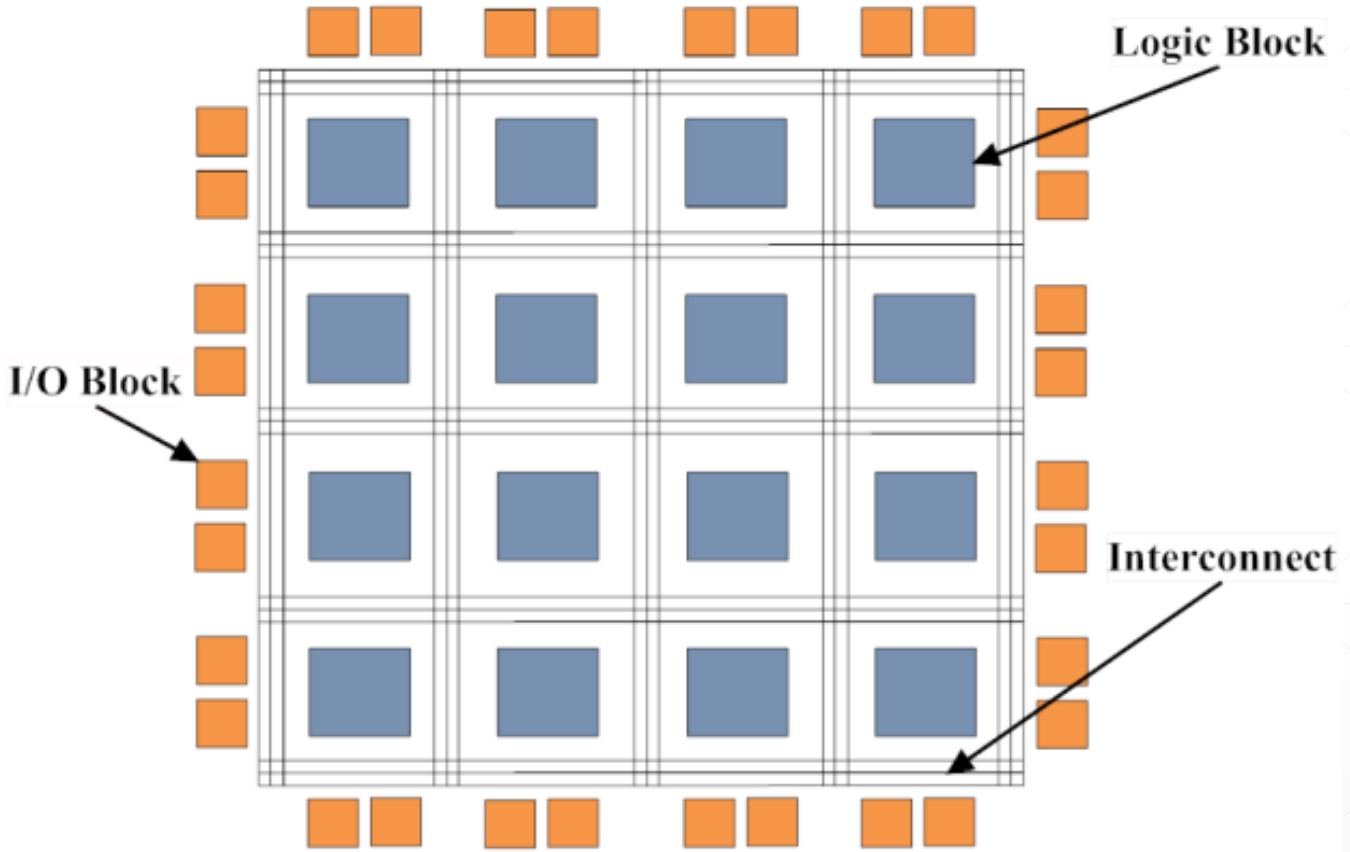
One custom AM ASIC version 09 will be able to store 384k patterns.

What is an FPGA

Field Programmable Gate Arrays (FPGAs) are semiconductor devices that are based on a matrix of configurable **logic blocks** connected via programmable **interconnects**, surrounded by **IO blocks**.

FPGAs can be **reprogrammed to desired application** or functionality requirements after manufacturing.

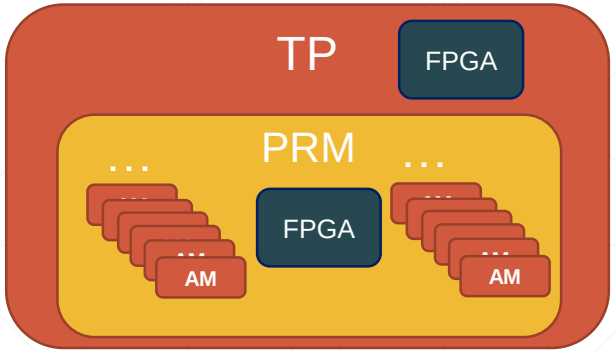


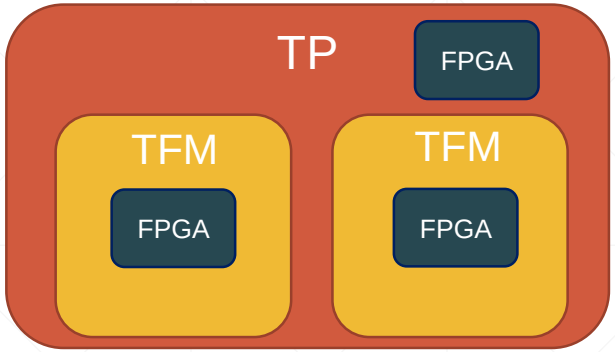


Where does it normally sit? On a board, e.g. a development kit. (Xilinx and Intel are the two major brands)

Carrier board and mezzanines

AMTP





SSTP

First Stage Fitting

- TP mezzanine forms clusters from the data coming from the ITk detector and send them to PRM.
- PRM does pattern recognition on the cluster from 8 layers to preliminary identify candidates of tracks.
- Chi square selection and parameter calculation then performed.
- Tracks and parameters are sent back to TP.

Second Stage Fitting

- Tracks and parameters can be sent to TFM.
- TFM performs extrapolation on the remaining 5 layers
- Chi square selection and parameter calculation performed on the complete tracks
- Tracks and parameters are sent back to TP.

HTT expected system size

Item	Number
Number of HTTIF PCs	24
Number of ATCA shelves for AMTP	48
Number of AMTP blades per shelf	12
Number of AMTP blades per HTTIF	24
Total number of AMTP	576
Number of PRM per AMTP	1
Total number of PRM	576
Number of AM ASIC per PRM	24
Total number of AM ASIC	13824
Number of ATCA shelves for SSTP	8
Number of SSTP blades per shelf	12
Number of SSTP blades per HTTIF	4
Total number of SSTP	96
Number of TFM per SSTP	2
Total number of TFM	192
Number of ConMon PCs per ATCA shelf	1
Total number of ConMon PCs	56