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Hardware-based track reconstruction for the ATLAS Trigger and Data Acquisition Phase-II system

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The Large Hadron Collider (LHC) at CERN announced the High-Luminosity LHC (HL-LHC) project in 2013 with the aim of increasing the machine performance for new physics discoveries. Researchers will take full advantage of HL-LHC to study known mechanisms in greater detail and observe rare new physics phenomena. HL-LHC poses some challenges on all the LHC experiments: a ten times higher readout rate at each collision. To fully exploit the physics potential, the ATLAS experiment will upgrade its Trigger and Data Acquisition (TDAQ) system.
A hardware processor dedicated to particle tracking, Hardware-based Track Trigger (HTT), will be installed in the ATLAS TDAQ system between 2024 and 2026. The goal of HTT is a fast reconstruction of charged particle tracks using a massively parallel architecture. The HTT algorithms are designed to exploit the computing power of modern Field Programmable Gate Arrays (FPGAs), popular for their flexibility in functionality and high-speed communication, and custom Associative Memory (AM) ASICs, performing pattern recognition. The board called Pattern Recognition Mezzanine (PRM) is the key component of the HTT system, where both a state-of-the-art FPGA and AM ASICs are mounted.

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