

Low charge noise in SiMOS quantum dots with full 300nm CMOS processes

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Silicon spin qubits have been considered as one of the most promising candidates for large scale quantum computers due to their long coherence times and compatibility with CMOS technology. However, the Si/SiO₂ interface, where the qubit stand, has been widely identified as the source for charge noise and disorder sites, which limits the qubit fidelity and scalability. We address this challenge by optimizing the gate stack with 300nm fabrication processes. On the fully integrated qubit structures, we characterize single electron transistors (SETs) across multiple devices and over large gate voltage range at milli-Kelvin temperatures and report notably low levels of charge noise below 1 $\mu\text{eV}/\sqrt{\text{Hz}}$. Moreover, the SET barriers show smooth pinch-off curves with highly uniform threshold voltages. These results underpin Si quantum dot qubit systems for large-scale quantum computing.

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