Contribution ID: **10** Type: **not specified**

Low charge noise in SiMOS quantum dots with full 300mm CMOS processes

Monday, 29 August 2022 12:10 (25 minutes)

Clement Godfrin [1], Asser Elsayed [1,2], Mohamed Shehata [1,2], Ruoyu Li [1], Stefan Kubicek [1], Shana Massar [1], Yann Canvel [1], Julien Jussot [1], Massimo Mongillo [1], Danny Wan [1], Pol van Dorpe [1,2], Kristiaan De Greve [1,3]
1 IMEC, Kapeldreef 75, B-3001 Leuven, Belgium
2 Department of Physics and Astronomy, KU Leuven, Celestijnenlaan 200D, B-3001 Leuven, Belgium
3 Department of Electrical Engineering, KU Leuven, Celestijnenlaan 200D, B-3001 Leuven, Belgium

Silicon spin qubits have been considered as one of the most promising candidates for large scale quantum computers due to their long coherence times and compatibility with CMOS technology. However, the Si/SiO2 interface, where the qubit stand, has been widely identified as the source for charge noise and disorder sites, which limits the qubit fidelity and scalability. We address this challenge by optimizing the gate stack with 300mm fabrication processes. On the fully integrated qubit structures, we characterize single electron transistors (SETs) across multiple devices and over large gate voltage range at milli-Kelvin temperatures and report notably low levels of charge noise below 1 μeV\/√Hz. Moreover, the SET barriers show smooth pinch-off curves with highly uniform threshold voltages. These results underpin Si quantum dot qubit systems for large-scale quantum computing.

Presenter: GODFRIN, Clément (IMEC Leuven)

Session Classification: Materials and large scale integration