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Deep Learning-Based Data Processing in Large-Sized Telescopes of the Cherenkov Telescope Array: FPGA Implementation and Comparison with GPUs

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The Large-Sized Telescopes (LSTs) are one of three telescope types being built as part of the Cherenkov Telescope Array Observatory (CTAO) to cover the lower energy range between 20 GeV and 200 GeV. The Large-Sized Telescope prototype (LST-1), installed at the Observatory Roque de Los Muchachos, La Palma, is currently being commissioned and has successfully taken data since November 2019. The construction of three more LSTs at La Palma is underway. A next generation camera that can be used in these three upcoming LSTs is being designed. One of the main challenges for the advanced camera is the 1GHz sampling rate generating 72 Tbps of data. A filter removing events caused by random coincidences from the night sky background or sensor noise shall reduce the data rate to 24 Gbps, corresponding to an event rate of approximately 30 kHz. Finally, a software stereo trigger, featuring deep learning inference on a high-speed Field Programmable Gate Array (FPGA), will further reduce the event rate to < 10 kHz.

To achieve such a large reduction, the different trigger levels are currently being developed for the implementation on FPGAs. This presentation focuses on porting the final trigger stage, a real-time deep learning algorithm, to FPGAs using two different approaches: the Intel AI Suite and the hls4ml packages. We compare the trade-offs obtained in FPGAs against running it in GPUs.

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