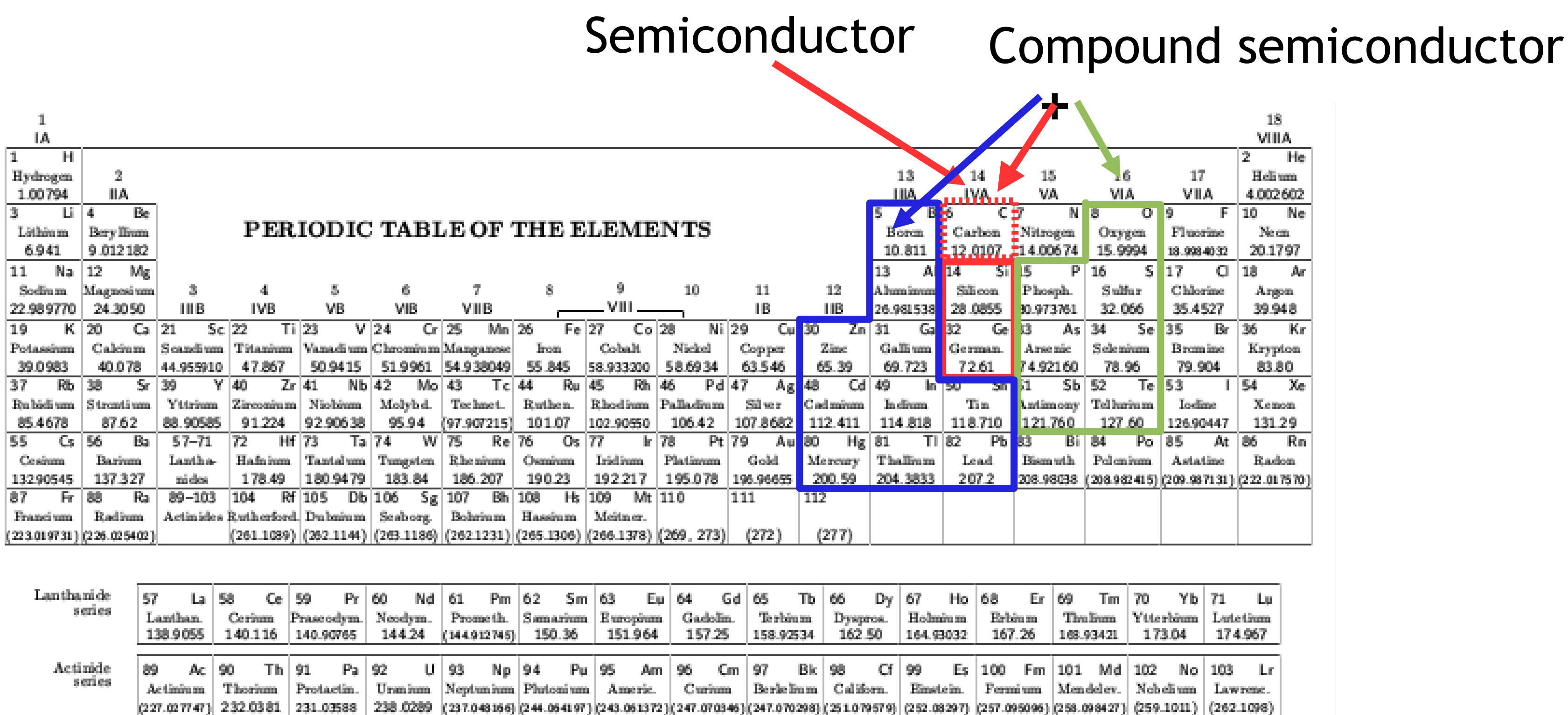
Lecture 2

- Introduction to semiconductors
- Structures and characteristics in semiconductors
    - Semiconductor p-n junction
    - Metal Oxide Silicon structure
    - Semiconductor contact

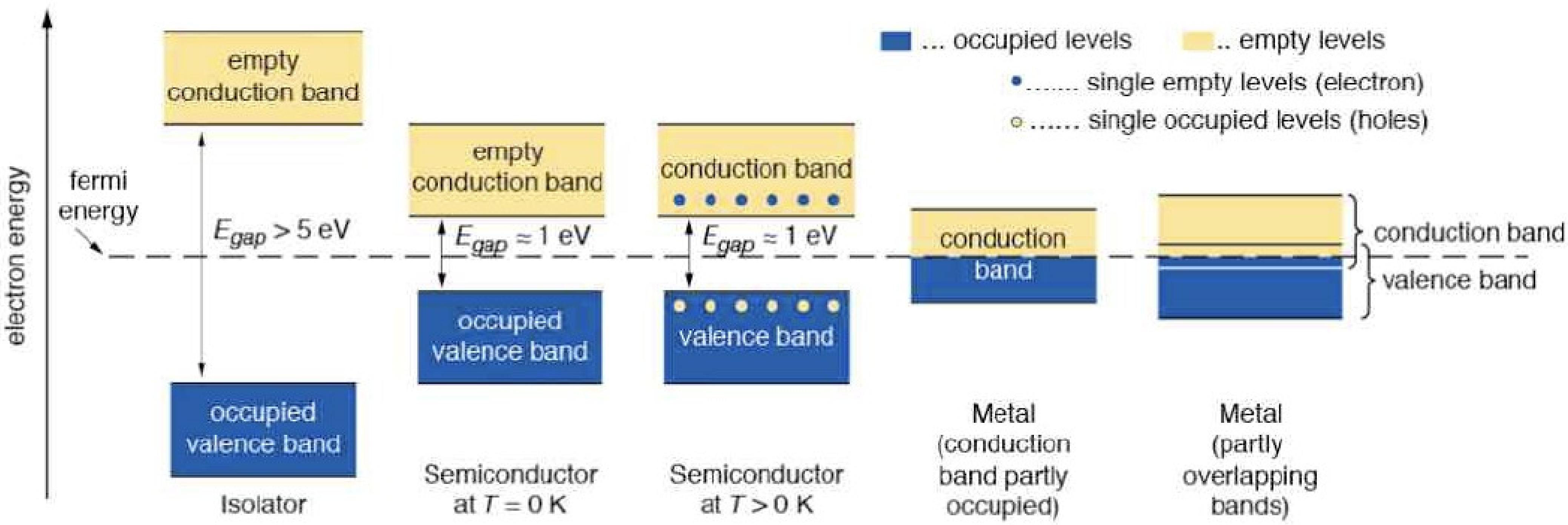
Literature

- Glen F. Knoll, Radiation Detection and Measurements, chapters 11,13,19
- Semiconductor Radiation Detectors, Gerhard Lutz, Springer-Verlag, 1999
- Nanohub tutorials

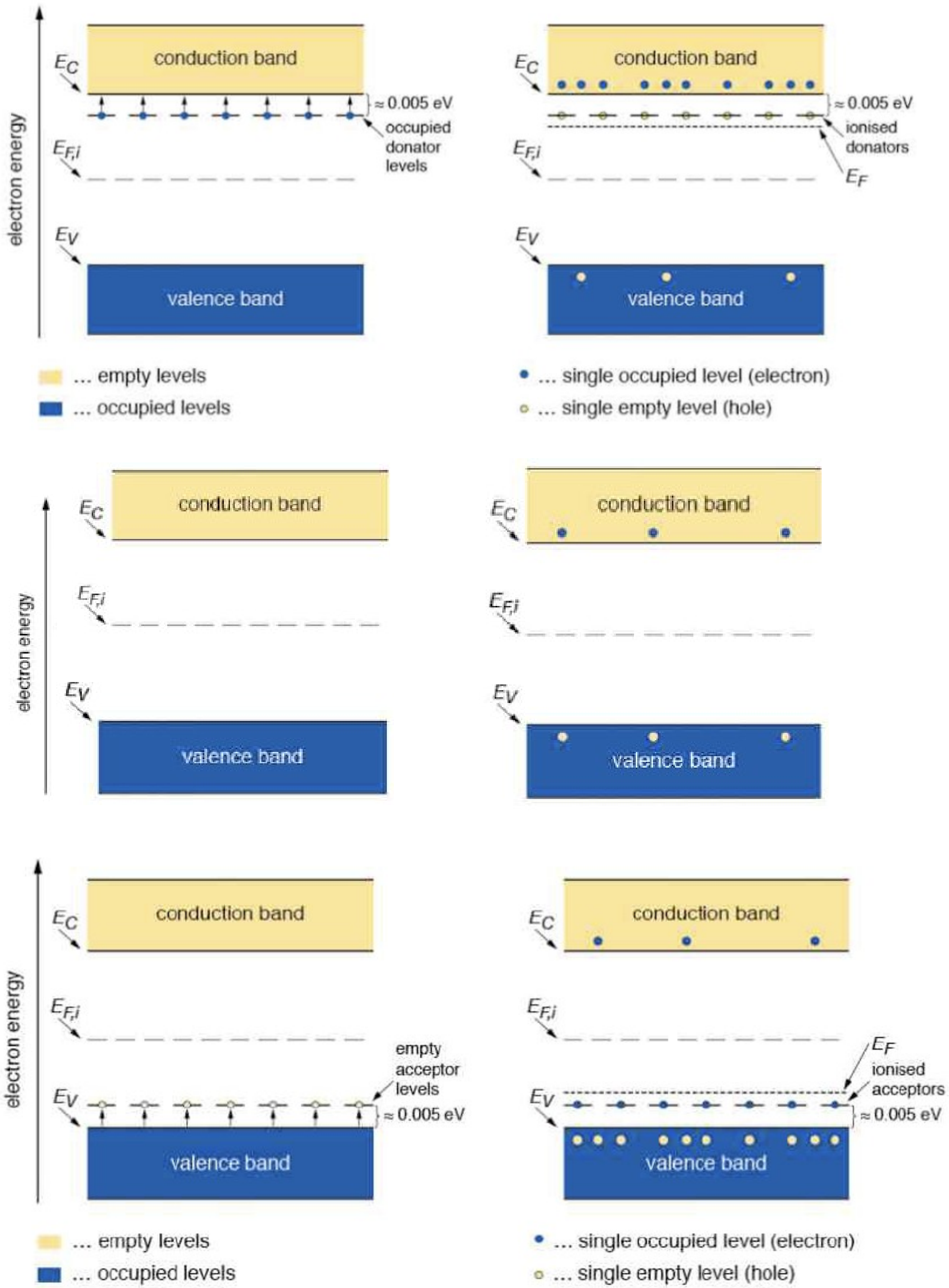
Elements used in semiconductor sensors



Basics on semiconductors



Semiconductor types



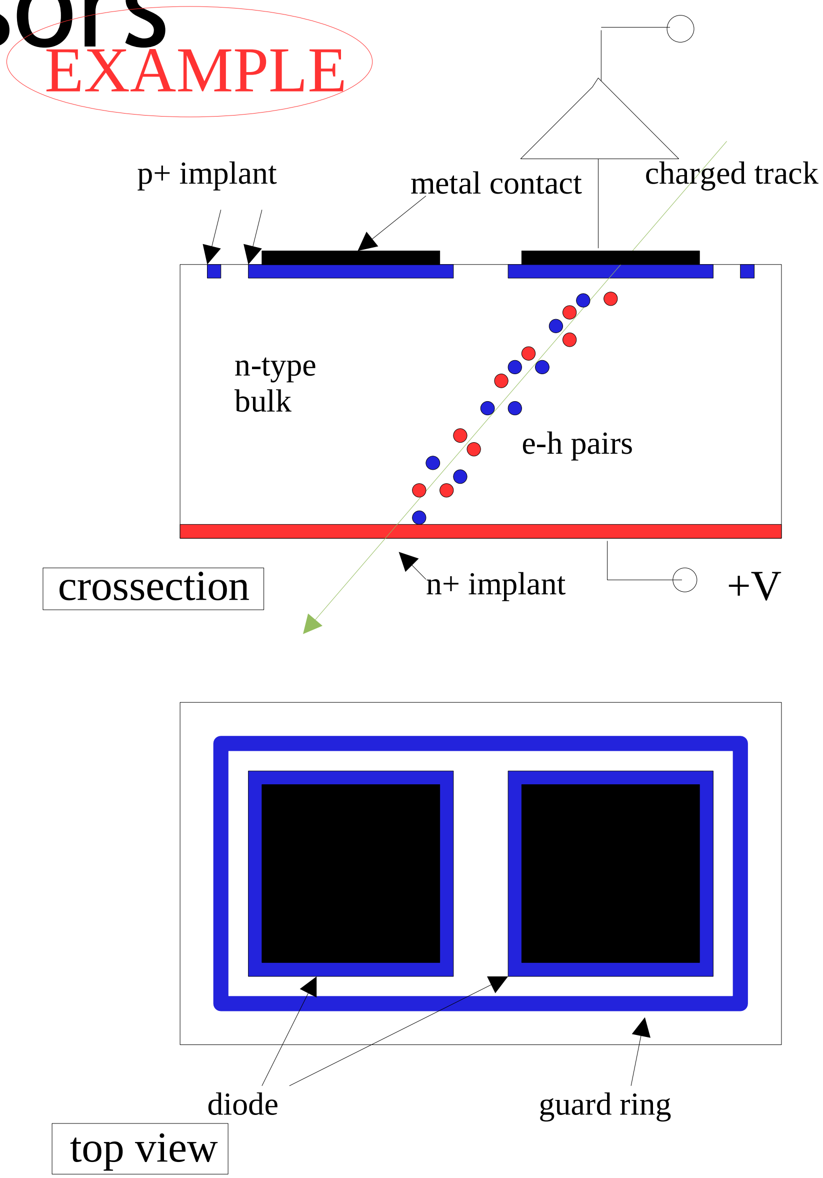
- n-type
  - ✔ Negative donor ions-> excess of electrons in conduction band
  - ✔ Doping with elements from VA,VIA
- Intrinsic
  - ✔ Equal amount of electrons in conduction band and holes in valence band
  - ✔ Pure silicon.
- p-type
  - ✔ Positive acceptor ions-> excess of holes in valence band
  - ✔ Doping with elements from IIA, IIIA

Properties of common semiconductors

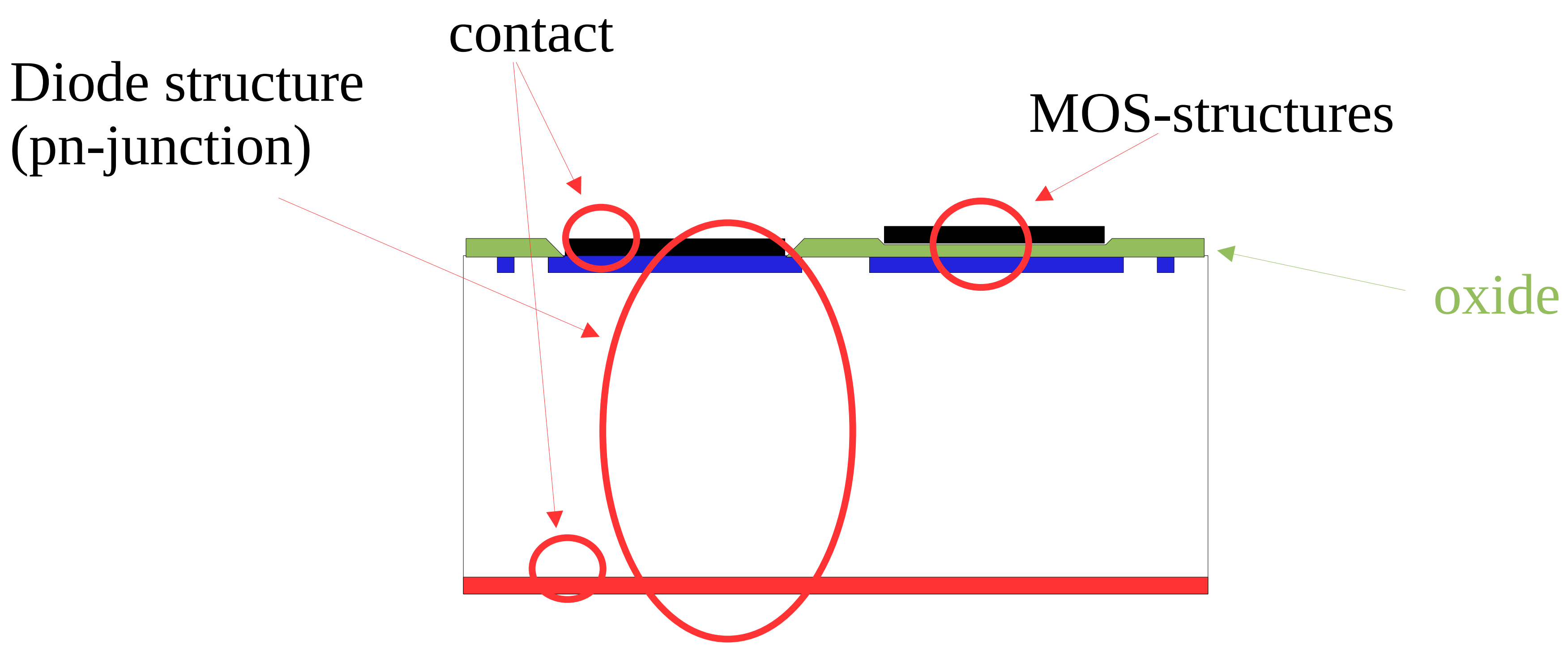
Substance	Si	Ge	GaAs	C	CdTe
Optical transition	Indirect	Indirect	Direct	Indirect	Direct
Energy gap [eV]	1.12	0.67	1.52	5.48	1.56
Intrinsic carrier concentration [cm^{-3}], n_i	1,5 x 10^{10}	2,4 x 10^{12}	2,1 x 10^{10}		
Mean energy for electron-hole pair creation [eV]	3.63	2.96	4.35	13.1	3.9
Drift mobility for electrons, μ_e [cm^2/Vs}	1350	3900	8800	1800	10500
Drift mobility for holes, μ_h[cm^2/Vs}	480	1900	320	1200	100
Intrinsic resistivity [Ω cm}	2,30 x 10^5	47			

Properties of semiconductor sensors

- ✔ Small band gap → large number of charge carriers per unit energy loss → excellent energy resolution
- ✔ High density compared with gaseous detectors
- ✔ High mobility → high speed
- ✔ Excellent material properties → rigidity, thermal
- ✔ Flexible to design
- ✔ Linearity and gain stability
- ✔ Tolerant to radiation
- ✔ High spatial resolution



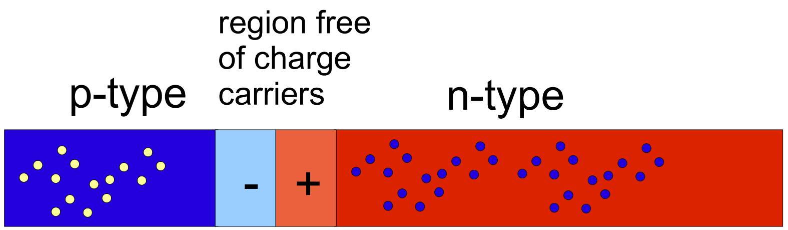
Structures in semiconductor sensors



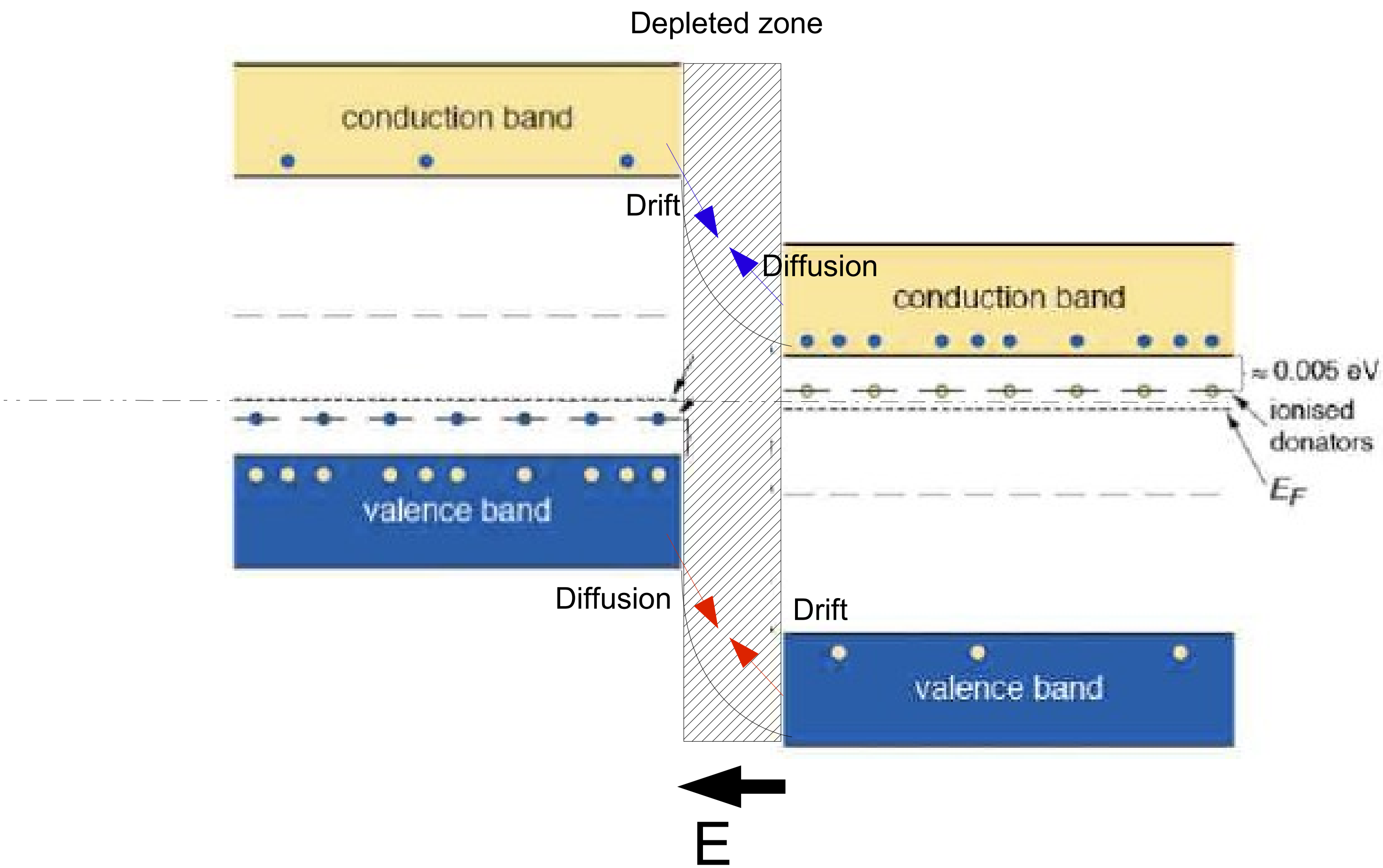
Most important and commonly used structures in semiconductor sensors are

- ✔ Diode structure, pn-junction and np-junction
- ✔ MOS structure (Metal-Oxide-Semiconductor)
- ✔ Contact (OHMIC,SCHOTTKY)

pn-junction

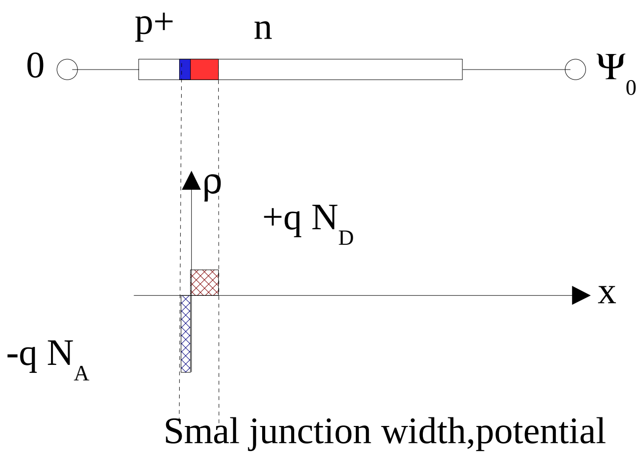


p-type
region free of charge carriers
n-type
-
+



Depleted zone
conduction band
Drift
Diffusion
conduction band
≈ 0.005 eV
ionised donators
E_F
valence band
Diffusion
Drift
valence band
E

Diode structure *(1 dimension)*



Study a typical n-bulk sensor structure:

Doping concentration in n-region (bulk) is low while the p-region has been implanted with high doping concentration. (Asymmetric junction)

$N_A >> N_D$

$$\Psi_0 = V_T \ln\left(\frac{N_A N_D}{n_i^2}\right)$$

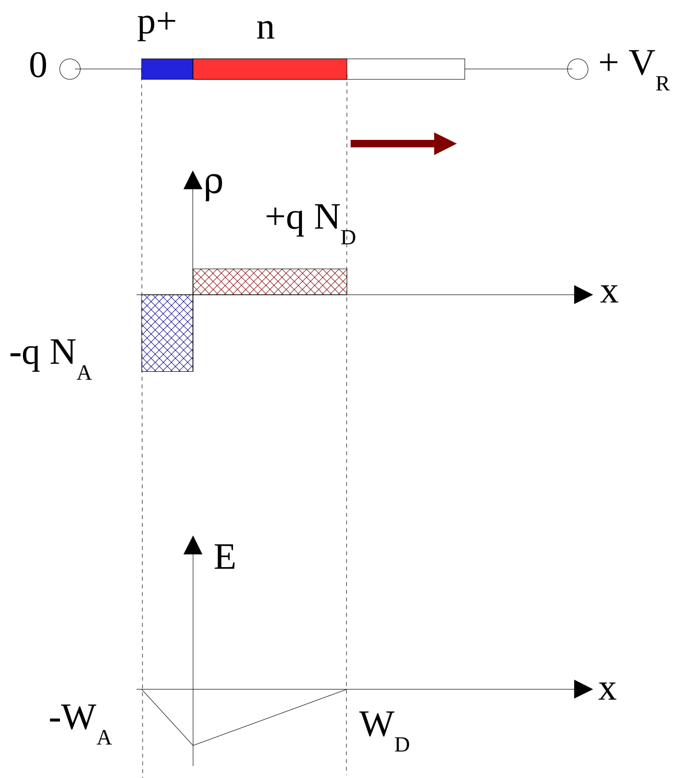
$$V_T = \frac{k_B T}{q} \approx 26\,mV$$

The built in potential (Ψ_0) in the junction is created by thermal diffusions of electrons into p-region and holes into n-region.

N_A, N_D = concentration of acceptor and donor ions.

n_i = concentration of charge carriers in the bulk (1.5E10 cm^{-3} for Silicon at 300K)

Diode structure (cont. 1)



If an external reverse bias voltage V_R is applied the junction will grow. The charge balance in the structure is maintained which results in:

$$W_A N_A = W_D N_D$$

For the region $-W_A$ to x=0 the potential across the region is described by the Poisson equation

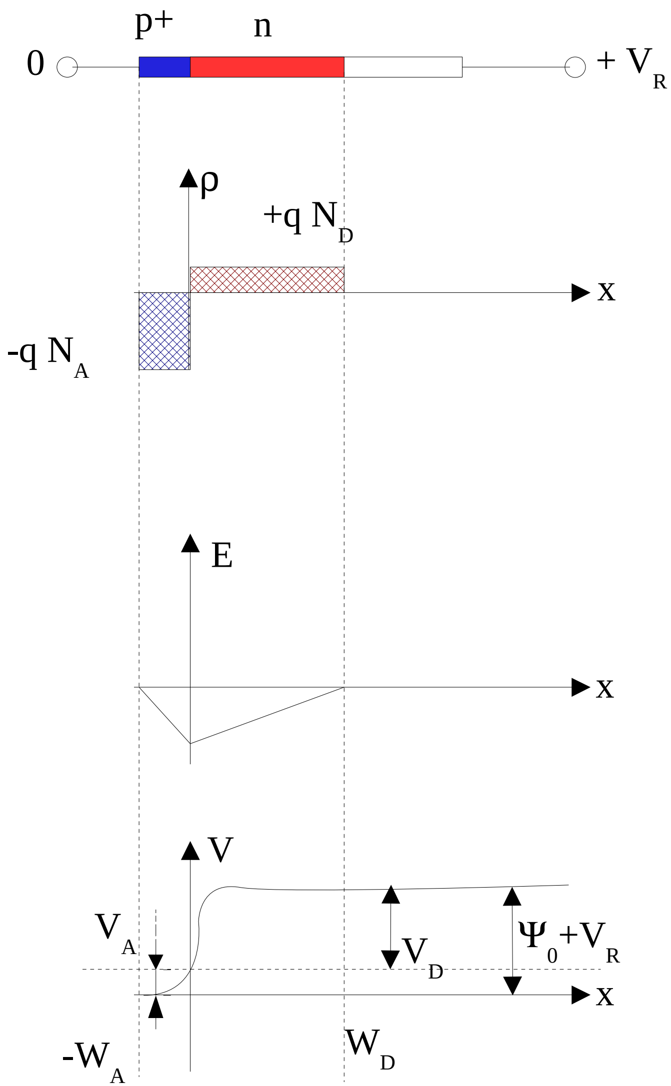
$$\frac{d^2V}{dx^2} = -\frac{\rho}{\epsilon_R \epsilon_0} = \frac{q N_A}{\epsilon_R \epsilon_0}$$

$$\boxed{E = -\frac{dV}{dx} = = -\frac{q N_A}{\epsilon_R \epsilon_0}(x + W_A)}$$

Integration over the p+ region and setting boundary condition $E(-W_A)=0$ results in the field in that region

Integration once more gives the potential in the region =>

Diode structure (cont. 2)



The potential in the region with boundary condition $V(-W_A) = 0$ becomes

$$V = \frac{q N_A}{\epsilon_R \epsilon_0}\left(\frac{x^2}{2} + W_A x + \frac{W_A^2}{2}\right)$$

$-W_A < x < 0$

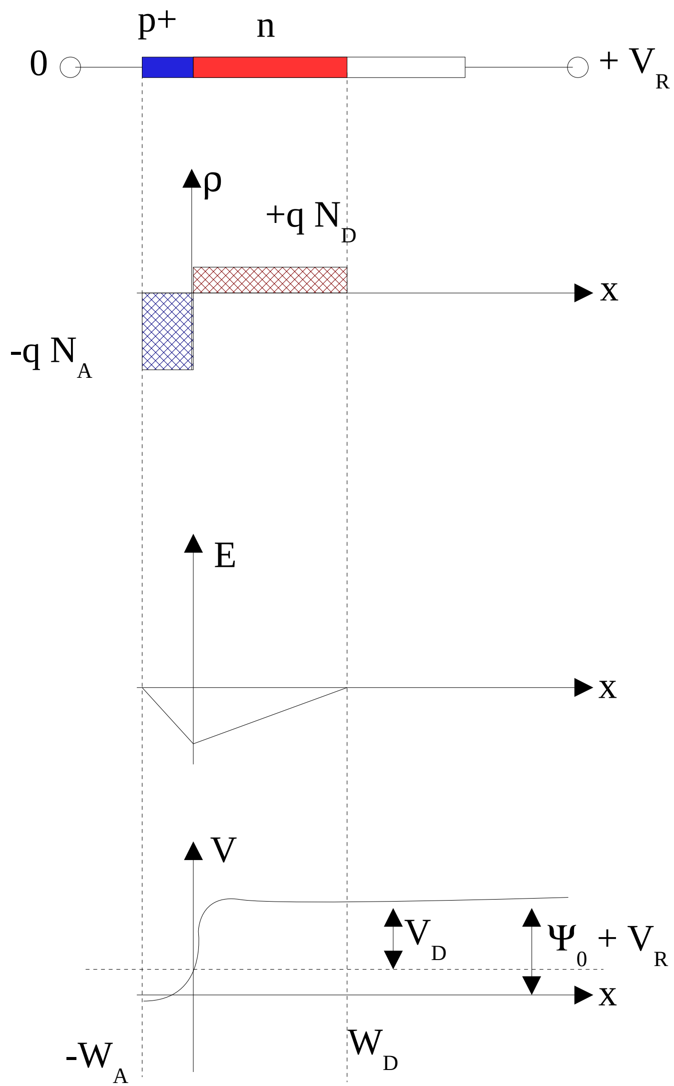
Use this expression to define the potentials V_A at x=0

$$V_A = \frac{q N_A}{\epsilon_R \epsilon_0} \frac{W_A^2}{2}$$

We can with similar considerations determine V_D at x=0

$$V_D = \frac{q N_D}{\epsilon_R \epsilon_0} \frac{W_D^2}{2}$$

Diode structure (cont. 3)



The total potential over the junction (with or without extra reverse bias) is

$$\Psi_0 + V_R = V_A + V_D$$

Because the junction is in equilibrium

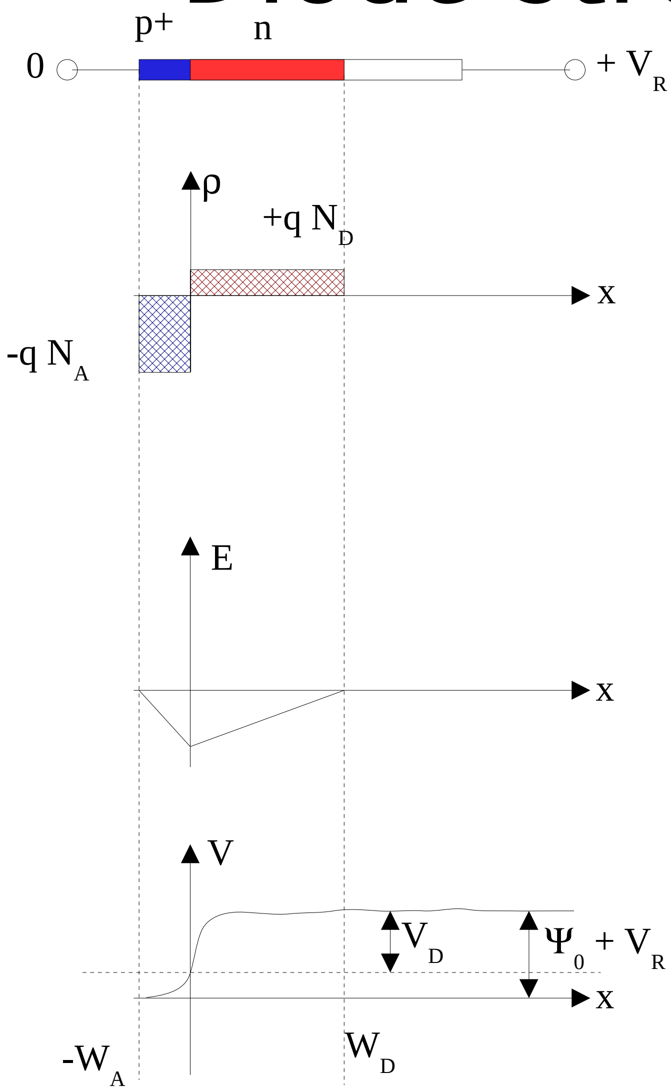
$$W_A N_A = W_D N_D$$

the expression can be written for the n-region

$$\Psi_0 + V_R = \frac{q W_D^2 N_D}{\epsilon_R \epsilon_0}\left(1 + \frac{N_D}{N_A}\right)$$

because of our geometry (n-bulk with shallow p+ implant) the only direction the depleted region can grow is in the n- region → $W_D >> W_A = W$

Diode structure (cont. 4)



$$W \approx W_D = \sqrt{\frac{\epsilon_R \epsilon_0 (\Psi_0 + V_R)}{q N_D \left(1 + \frac{N_D}{N_A}\right)}}$$

SUMMARY:

•Depletion width is proportional to the square root of the reverse bias voltage.

•More doping in bulk gives less depletion layer → more voltage will be needed to give same *W*.

•When W_D reaches the physical end of the n-bulk (back plane) the sensor is <u>fully depleted</u>.

Important features

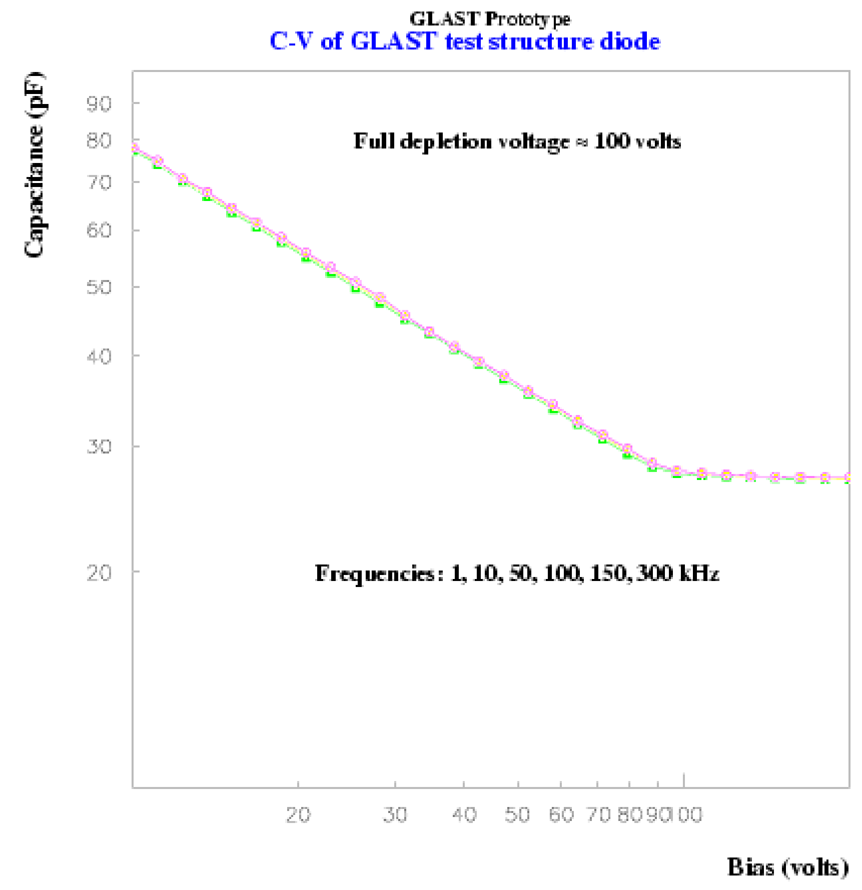
- Macroscopic features of a good semiconductor sensor are
  - ✔ Low capacitive load → low noise in readout electronics
  - ✔ Low leakage current → low noise in readout electronics
  - ✔ Good charge collection
  - ✔ High speed

Characteristics of the diode structure

- **Capacitance (C-V)**

The capacitance of the diode influences the noise of the readout electronics by loading the amplifier *(will be discussed later in this series)*. The capacitance of the pn-junction is given by

$$C_j = \frac{\epsilon_R \epsilon_0}{W_D}$$



The capacitance of the junction will decrease when reverse bias voltage is applied until full depletion is reached.

WE WANT LOW CAPACITANCE!

Characteristics of the diode structure

- **Leakage current (I-V)**
  - ✔ <u>diffusion current</u>

Electrons generated in the p+ region and holes generated in the n+ region diffuse to the junction and are collected by electrodes. Small effect for Si but large for Ge at room temperature.

$$J_s = q\sqrt{\frac{D_P}{\tau_P}}\frac{n_i^2}{N_D}$$

where D_P is the diffusion constant for electrons in the p+ region and τ_P is the lifetime of the electron

- ✔ <u>generating current</u>

This is the dominated current in a good sensor. The current is due to generation-recombination in the depleted region.

$$J_g = q\,gW$$

g is the generation rate dependent of the intrinsic carrier concentration, n_i.

$$g = \frac{n_i}{\tau_g}$$

τ_g is the generation lifetime ($\sim 10^{-3}$ s)

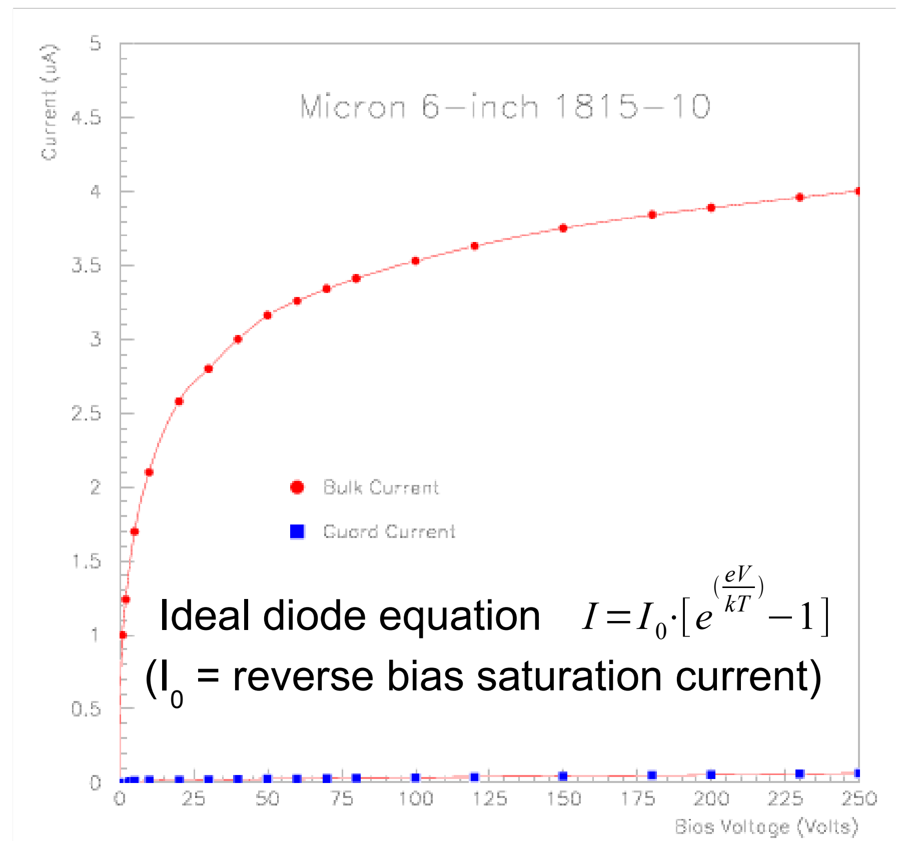
Characteristics of the diode structure

- **Leakage current (I-V)**
  - ✔ <u>generating current(cont.)</u>

    The current is also sensitive to temperature. 8K increase in temperature doubles the current!!

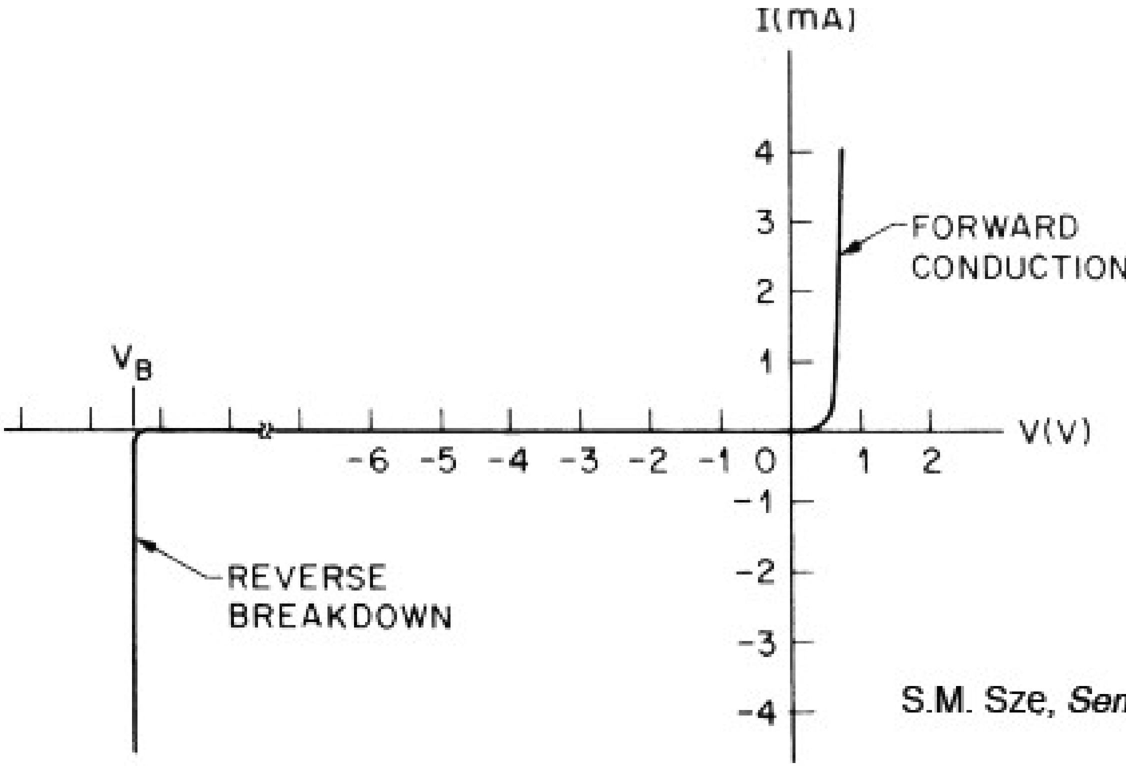
  - ✔ <u>surface current</u>

    Surface current is a contribution on complex effects happening in the boarder between the semiconductor and surface oxide. The current level is very dependent on processing quality and handling.

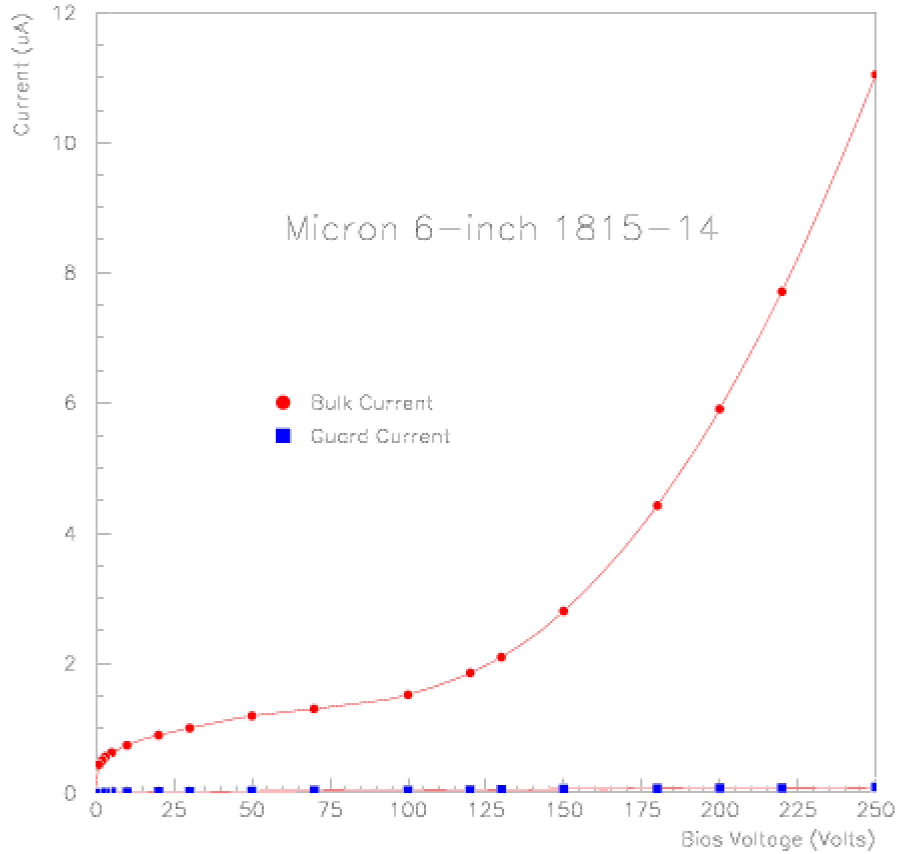


GOOD I-V curve

More on IV-characteristics

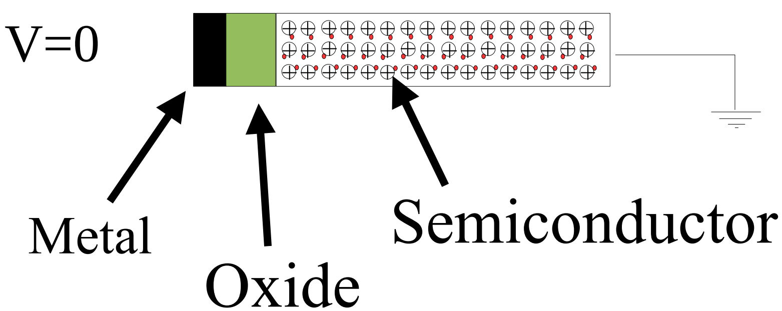


S.M. Sze, *Semiconductor Devices* , J. Wiley & Sons, 1985


Micron 6−inch 1815−14
Bulk Current
Guard Current
Current (uA)
Bias Voltage (Volts)
0
2
4
6
8
10
12
0
25
50
75
100
125
150
175
200
225
250

BAD I-V curve !

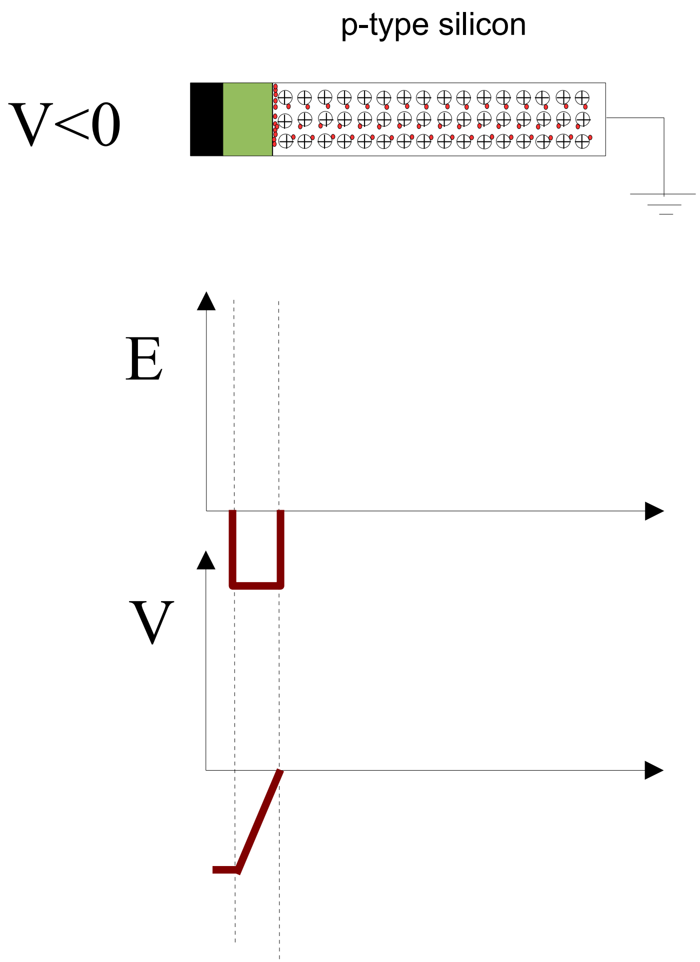
Metal-Oxide-Semiconductor structure



- MOS structure (or more general Metal-Insulator-Semiconductor, MIS) is widely used in electronics industry to make gates and in sensor industry to make AC-coupled sensors

- The figure shows a 1-dimensional picture of a MOS structure with a n-doped semiconductor insulated from a metal layer with a oxide.
- If the potential at the metal is at the same potential as the semiconductor and the charge carrier electrons in the n-type semiconductor will be homogeneously distributed → no field across the oxide. This is called the <u>Flat Band condition</u>.

MOS in accumulation



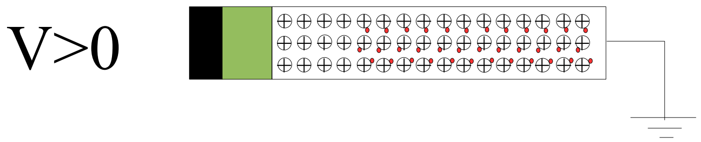
- If the potential on the metal is set below the voltage of the semiconductor the holes are attracted to the semiconductor-oxide interface where they accumulate to a very thin layer. This is called <u>Accumulation condition.</u>

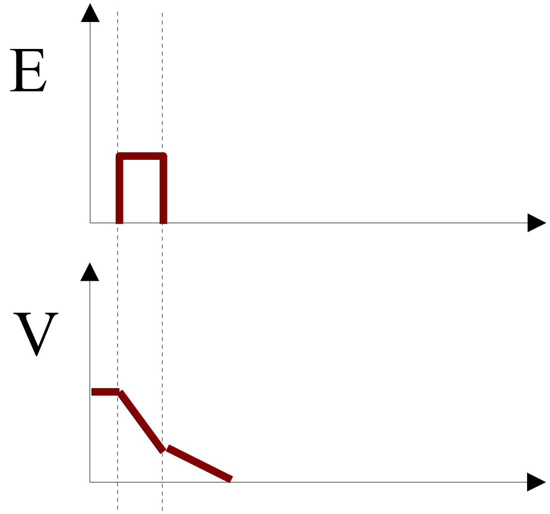
- A field is created across the oxide.

$$E_{ox} = \frac{Q_{acc}}{\epsilon_{ox}\epsilon_0}$$

$$V = E_{ox} d_{ox} = -\frac{Q_{acc}}{C_{ox}}$$

MOS in depletion



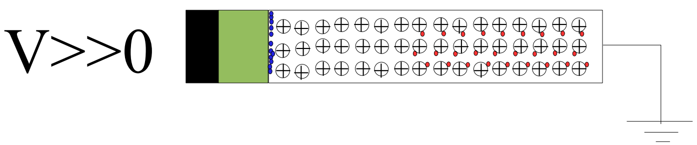


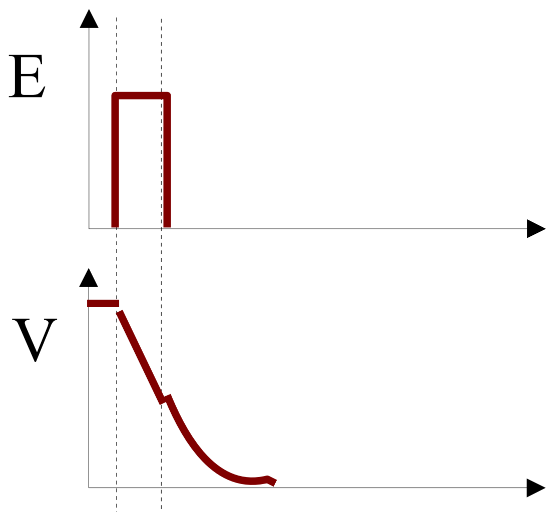
- If the potential on the metal is increased slightly above the voltage of the semiconductor the holes are repelled from the semiconductor-oxide interface and a negative space charge region is formed. This is called <u>Depletion condition</u> *(used by CCD detectors)*
- A field is created across the oxide and the space charge regions.

$$E_{ox} = -\frac{q N_D}{\epsilon_{ox} \epsilon_0} d_s$$

$$E_s = -\frac{q N_D}{\epsilon_s \epsilon_0} d_s$$

MOS in inversion





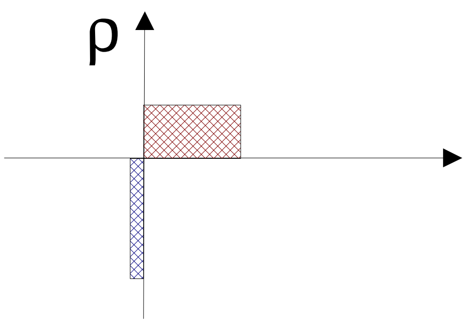
- If the potential on the metal is very much above the voltage of the semiconductor the holes are pushed even further away from the semiconductor-oxide interface. Thermally generated electron-holes pairs are separated from each other thus an inversion layer of electrons is built up at the interface. This is called <u>Inversion condition.</u>

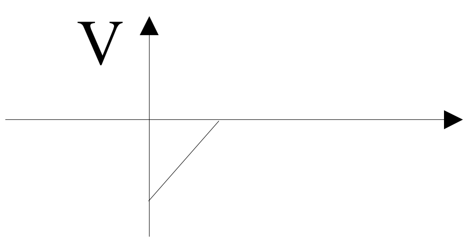
$$E_{ox} = -\frac{q N_D}{\epsilon_{ox} \epsilon_0} d_{max} - \frac{Q_{inv}}{\epsilon_{ox} \epsilon_0}$$

$$E_s = -\frac{q N_D}{\epsilon_s \epsilon_0} d_s$$

Schottky contact

- A contact to the semiconductor can be made by deposition of a metal layer directly onto the silicon. This metal-semiconductor contact was one of the first practical semiconductor showing rectifying properties, the Schotky contact (used in surface barrier detectors).
- If the doping concentration under the metal is high the characteristic resistance of the junctions becomes small, the rectifying feature turns into an Ohmic contact.





END LECTURE