



FYSIKUM

# Introduction to Programmable Logic

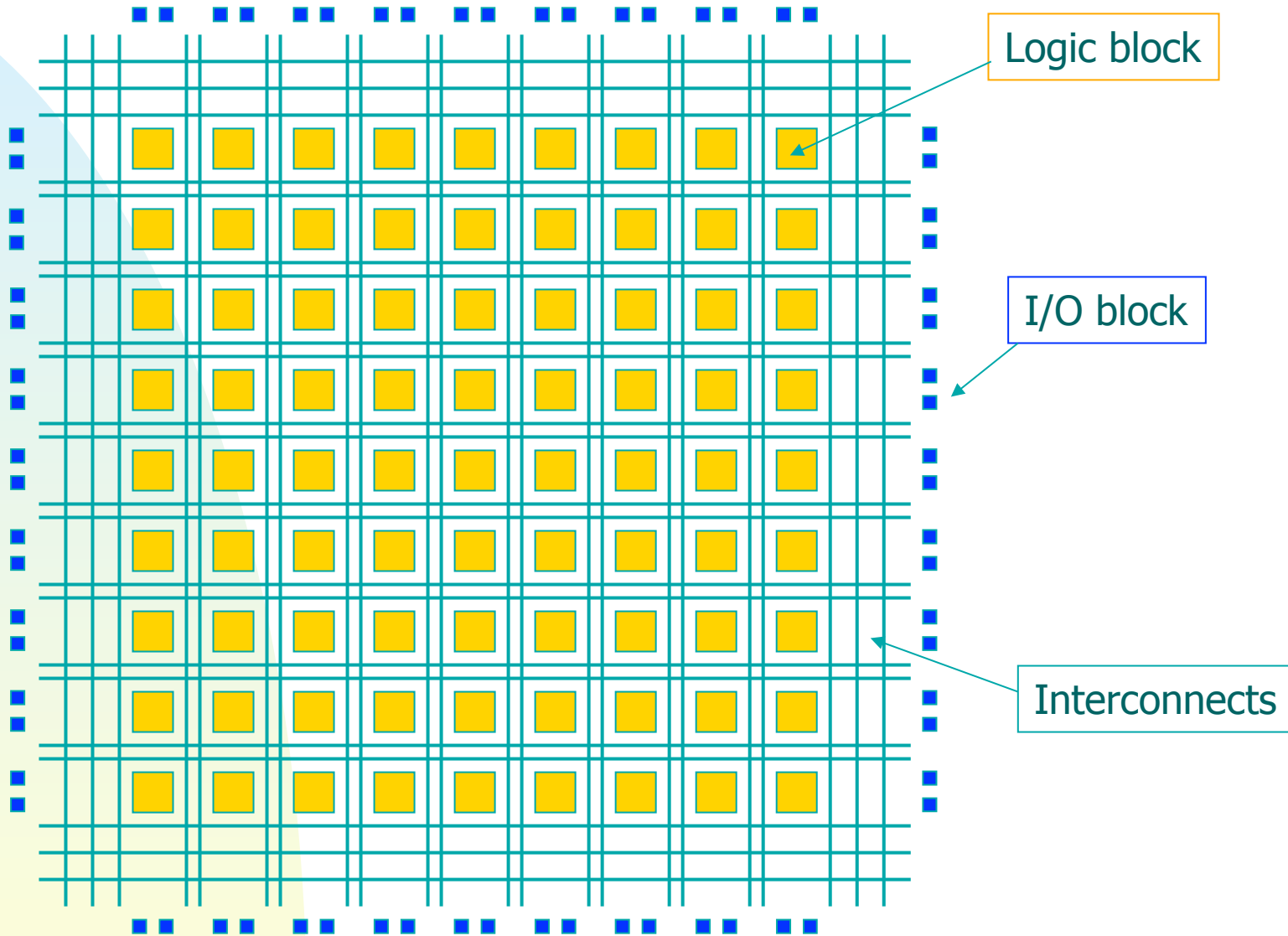
Nordic detector school

FPGA introduction

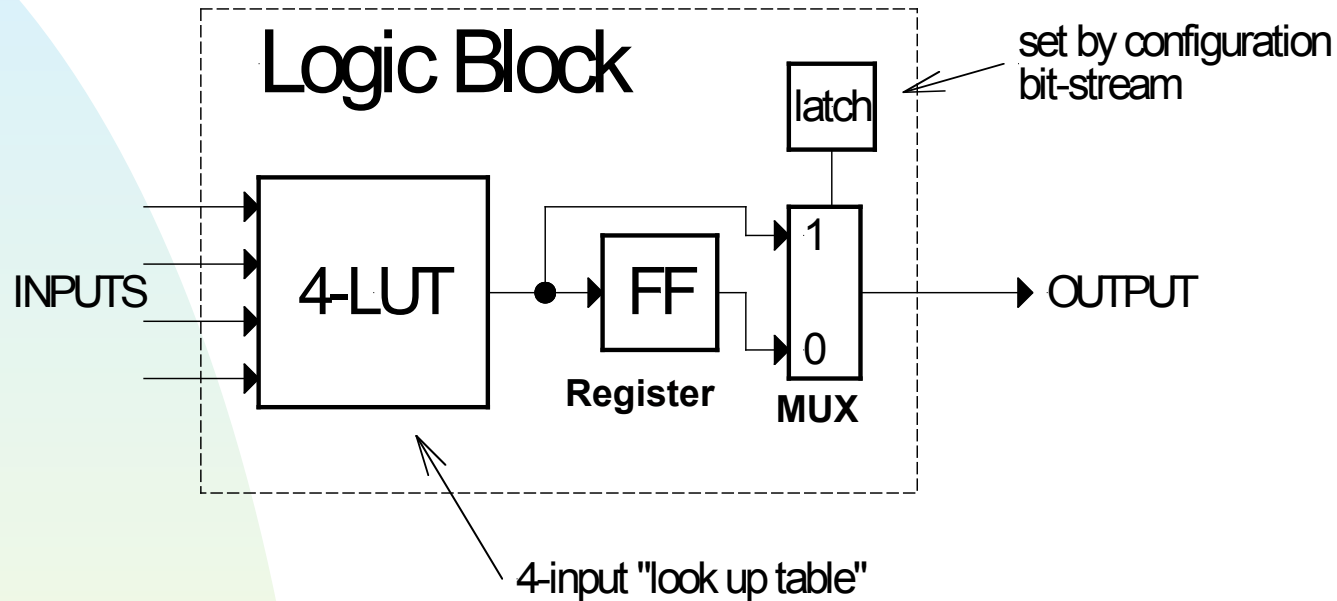
Introduction to VHDL

Implementation design flow

# FPGA Structure



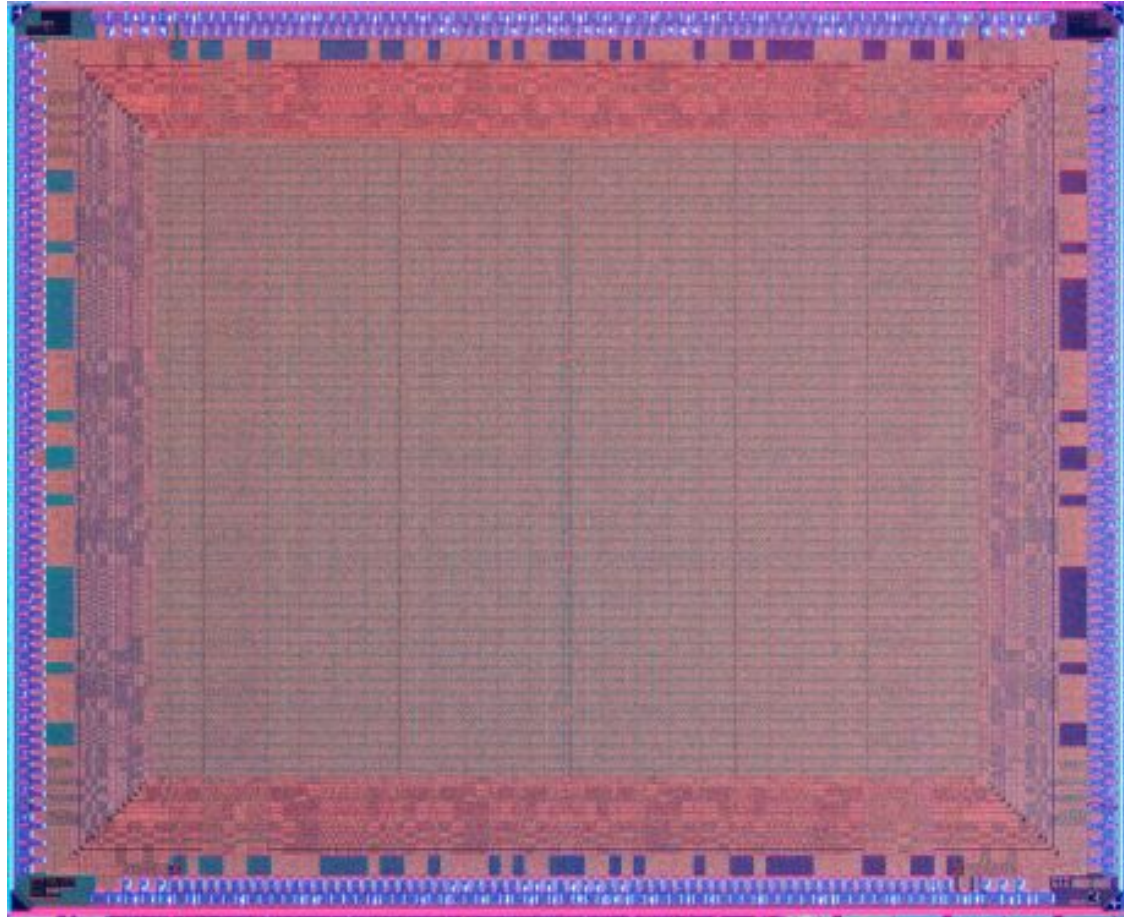
# FPGA Logic Block (idealized)



- 4-input *look up table (LUT)*
  - ◆ implements combinatorial logic
- Register
  - ◆ optionally stores output of LUT

# Field-Programmable Gate Arrays

- Xilinx Spartan-3 die image. Note the regularity



# Other FPGA features:

- Dedicated block memories
  - ◆ Dual-port static RAM
- Digital clock management/synthesis
- Dedicated multipliers
  - ◆ Important for digital signal processing
- "Hard" CPU cores
  - ◆ Xilinx: PowerPC, ARM 9
  - ◆ Altera: Nios (Stratix II)
- Multi-Gbit transceivers

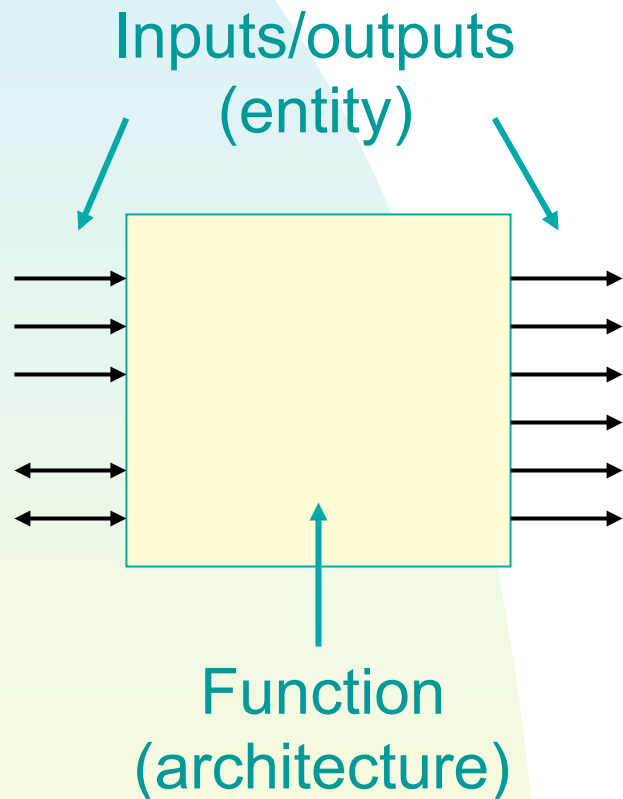
# For this course:

- Device: Xilinx FPGA (Spartan 3E)
- Design language: VHDL
- Simulation tool: Xilinx iSim
- Implementation: Xilinx ISE
  
- These are specific choices, but....
  - ◆ Overall contents are similar to other environments
  - ◆ Not very difficult to transfer skills

# VHDL introduction

- **VHSIC Hardware Description Language**
  - ◆ (VHSIC: Very high speed integrated circuit)
- Both concurrent and sequential operations
- International standard (1987, 1993, 2002)
  - ◆ Pure language definition
- Large standard, with multiple ways to code the same behavior

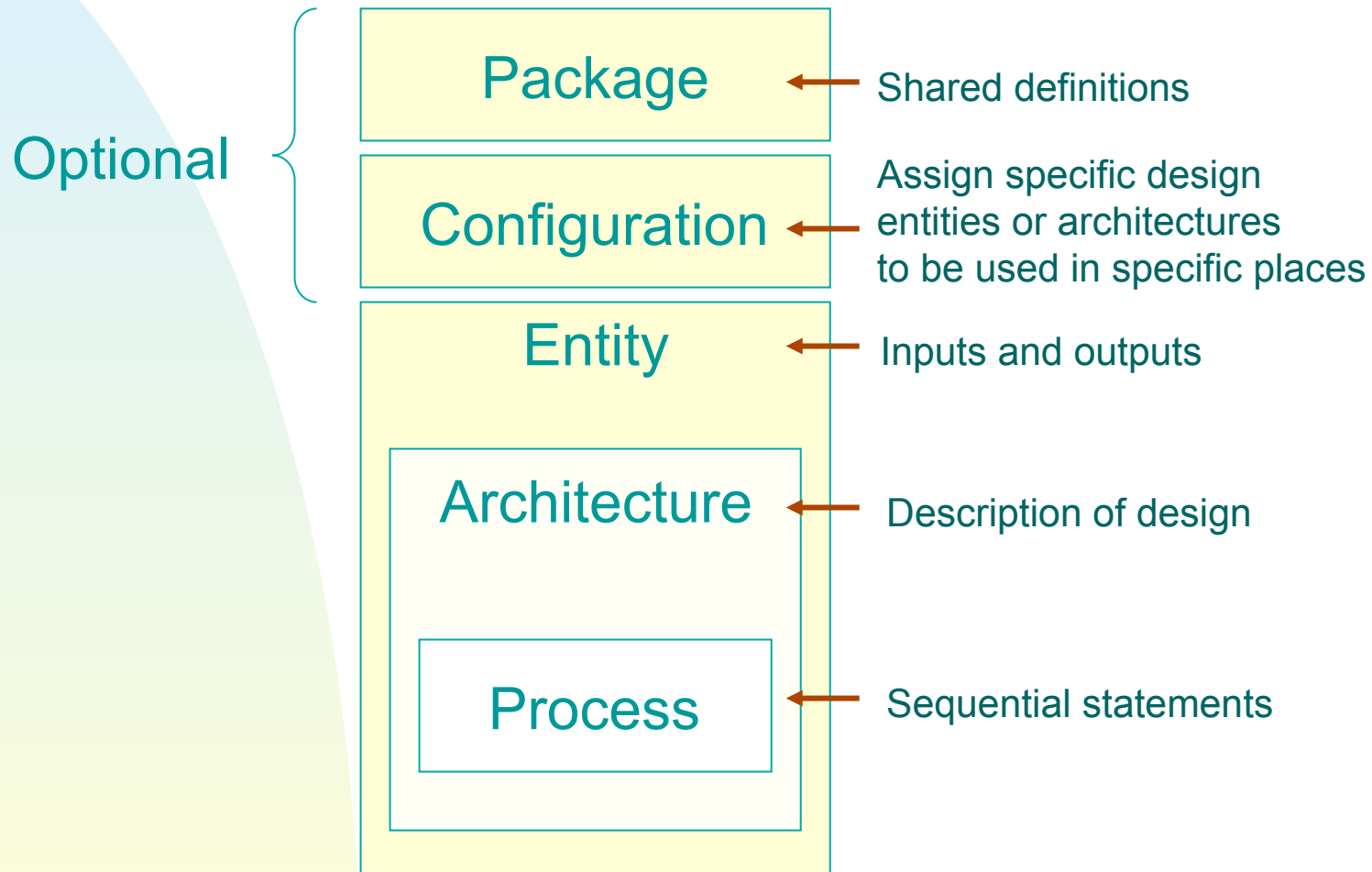
# Design unit (library unit)



- In most basic form, defines
  - ◆ Inputs/outputs (entity)
  - ◆ Function of unit (architecture)
- Can be instantiated and connected together in higher level design units.



# VHDL design unit



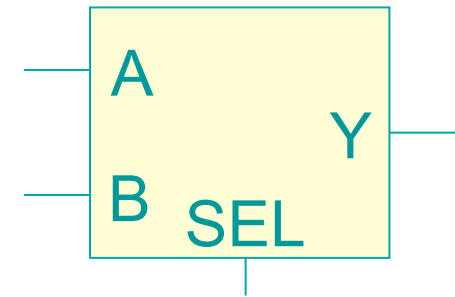
# Multiplexer entity

```
library ieee;  
use ieee.std_logic_1164.all;  
  
entity Mux is  
port (  
    a:    in  std_logic;  
    b:    in  std_logic;  
    sel:  in  std_logic;  
    y:    out std_logic  
);  
end Mux;
```

Port name

Direction

Type

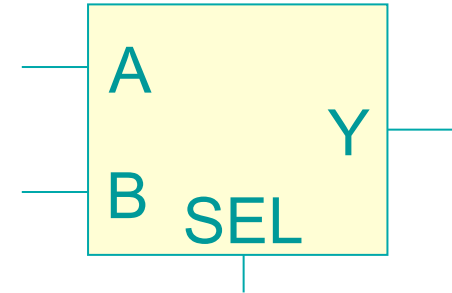


no semicolon  
after last port  
declaration!

# An architecture

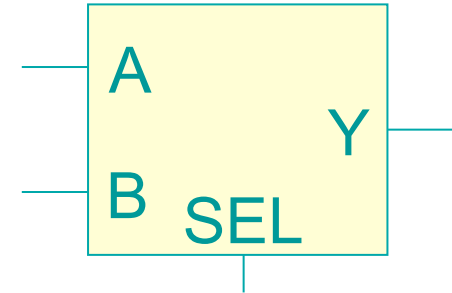
(many ways to do this)

```
architecture arch3 of Mux is
begin
    y <= a when sel='0' else b;
end arch3;
```



# Complete design unit:

```
--  
-- A 2 input multiplexer circuit  
--  
library ieee;  
use ieee.std_logic_1164.all;  
  
entity Mux is  
port(  a:      in std_logic;  
       b:      in std_logic;  
       sel:    in std_logic;  
       y:      out std_logic  
);  
end Mux;  
  
architecture arch2 of Mux is  
begin  
    y <= a when sel='0' else b;  
  
end arch2;
```



# Xilinx design environment (ISE)

The screenshot displays the Xilinx ISE Project Navigator interface. The main window shows a Design Overview with a tree view of the design hierarchy and a list of reports. The Design Overview includes sections for Design Overview, Errors and Warnings, and Detailed Reports. The Design Overview section is expanded to show a list of reports, including Summary, IOB Properties, Module Level Utilization, Timing Constraints, Pinout Report, Clock Report, Static Timing, Translation Messages, Map Messages, Place and Route Messages, Timing Messages, Bitgen Messages, and All Implementation Messages. The Detailed Reports section is also expanded to show the Synthesis Report.

The Device Utilization Summary table is displayed on the right side of the interface. The table has the following columns: Logic Utilization, Used, Available, Utilization, and Note(s). The table contains the following data:

Logic Utilization	Used	Available	Utilization	Note(s)
Number of Slice Flip Flops	1,097	11,776	9%	
Number of 4 input LUTs	999	11,776	8%	
Number of occupied Slices	976	5,888	16%	
Number of Slices containing only related logic	976	976	100%	
Number of Slices containing unrelated logic	0	976	0%	
Total Number of 4 input LUTs	1,184	11,776	10%	
Number used as logic	793			
Number used as a route-thru	185			
Number used for Dual Port RAMs	188			
Number used as Shift registers	18			
Number of bonded IOBs	91	372	24%	
IOB Flip Flops	55			
Number of ODDR2s used	41			
Number of BUFGMUXs	8	24	33%	
Number of DCMs	2	8	25%	
Number of RAMB16BWEs	3	20	15%	
Average Fanout of Non-Clock Nets	3.40			

The Console window at the bottom of the interface shows the following output:

```
grf.rf/gntv_or_sync_fifo.mem/gbm.gbmga.ngecc.bmg/blk_mem_generator/valid
.cstr/ramloop[0].ram.r/s3_noinit.ram/dpram.dp36x18.ram>:<RAMB16BWE_RAMB16BWE>
.
WARNING:PhysDesignRules:812 - Dangling pin <DOB31> on
block:<VGAD_Cntrlr_inst/camd_afifo_inst/U0/xst_fifo_generator/gcon
grf.rf/gntv_or_sync_fifo.mem/gbm.gbmga.ngecc.bmg/blk_mem_genera
```

So, how do you use it?

# Create a new project

**Create New Project**

Specify project location and type.

Enter a name, locations, and comment for the project

Name:

Location:  ...

Working Directory:  ...

Description:

Select the type of top-level source for the project

Top-level source type:

# Select device, design flow

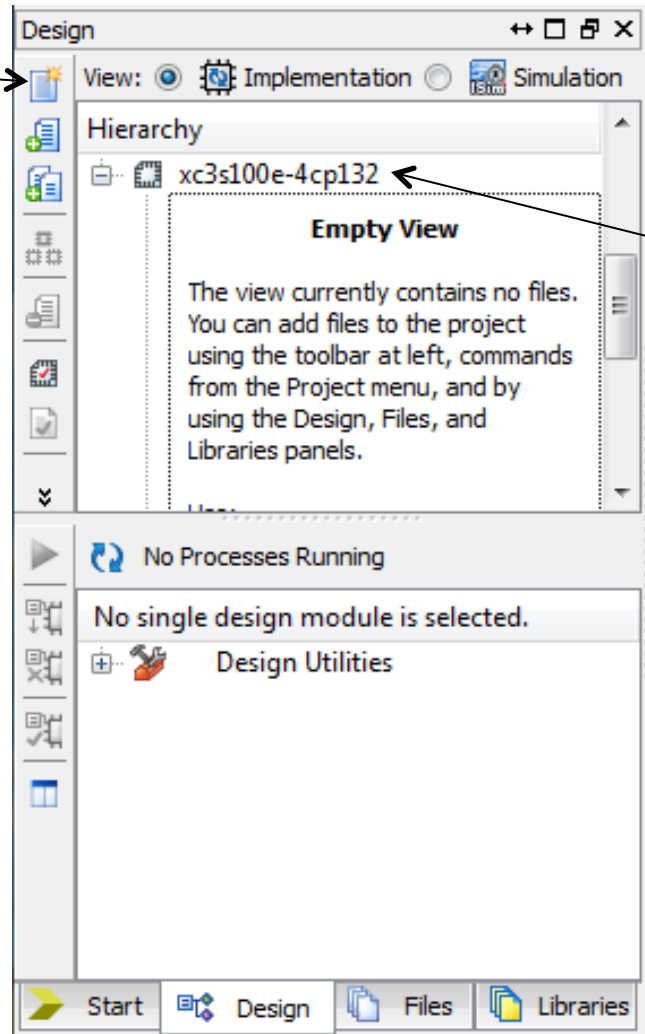
**Project Settings**

Specify device and project properties.  
Select the device and design flow for the project

Property Name	Value
Evaluation Development Board	None Specified
Product Category	All
<b>Family</b>	Spartan3E
Device	XC3S100E
Package	CP132
Speed	-4
Top-Level Source Type	HDL
Synthesis Tool	XST (VHDL/Verilog)
Simulator	ISim (VHDL/Verilog)
Preferred Language	VHDL
Property Specification in Project File	Store non-default values only
Manual Compile Order	<input type="checkbox"/>
VHDL Source Analysis Standard	VHDL-93
Enable Message Filtering	<input type="checkbox"/>

# Create new source

Click here



Or right-click here for menu



# New source options

Select Source Type

Select source type, file name and its location.

- IP (CORE Generator & Architecture Wizard)
- Schematic
- User Document
- Verilog Module
- Verilog Test Fixture
- VHDL Module
- VHDL Library
- VHDL Package
- VHDL Test Bench
- Embedded Processor

File name:  
mux\_2bit

Location:  
C:\Users\silver\VHDL\multiplexer

Add to project

More Info Next Cancel

# Initial definitions

**Define Module**

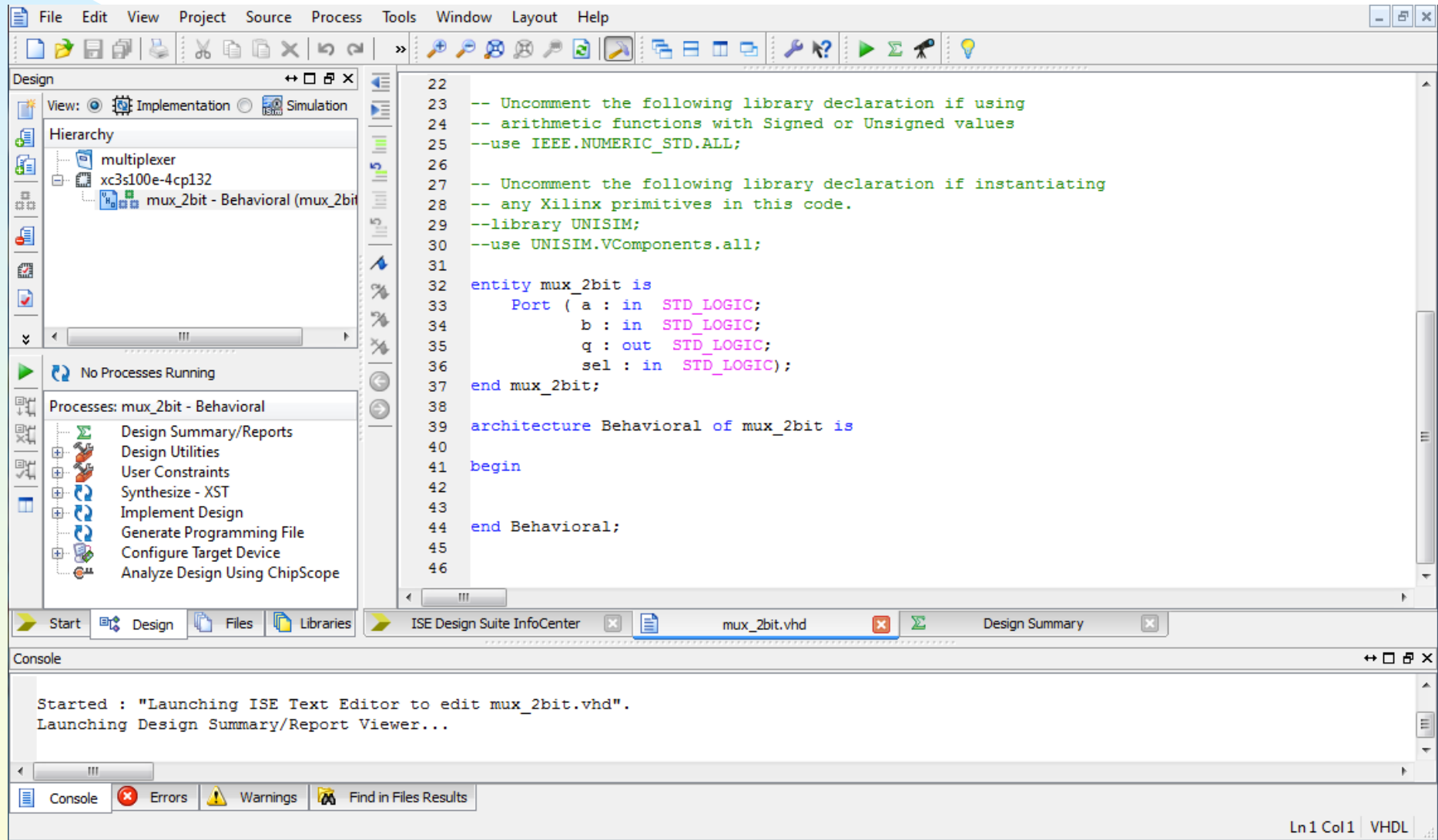
Specify ports for module.

Entity name

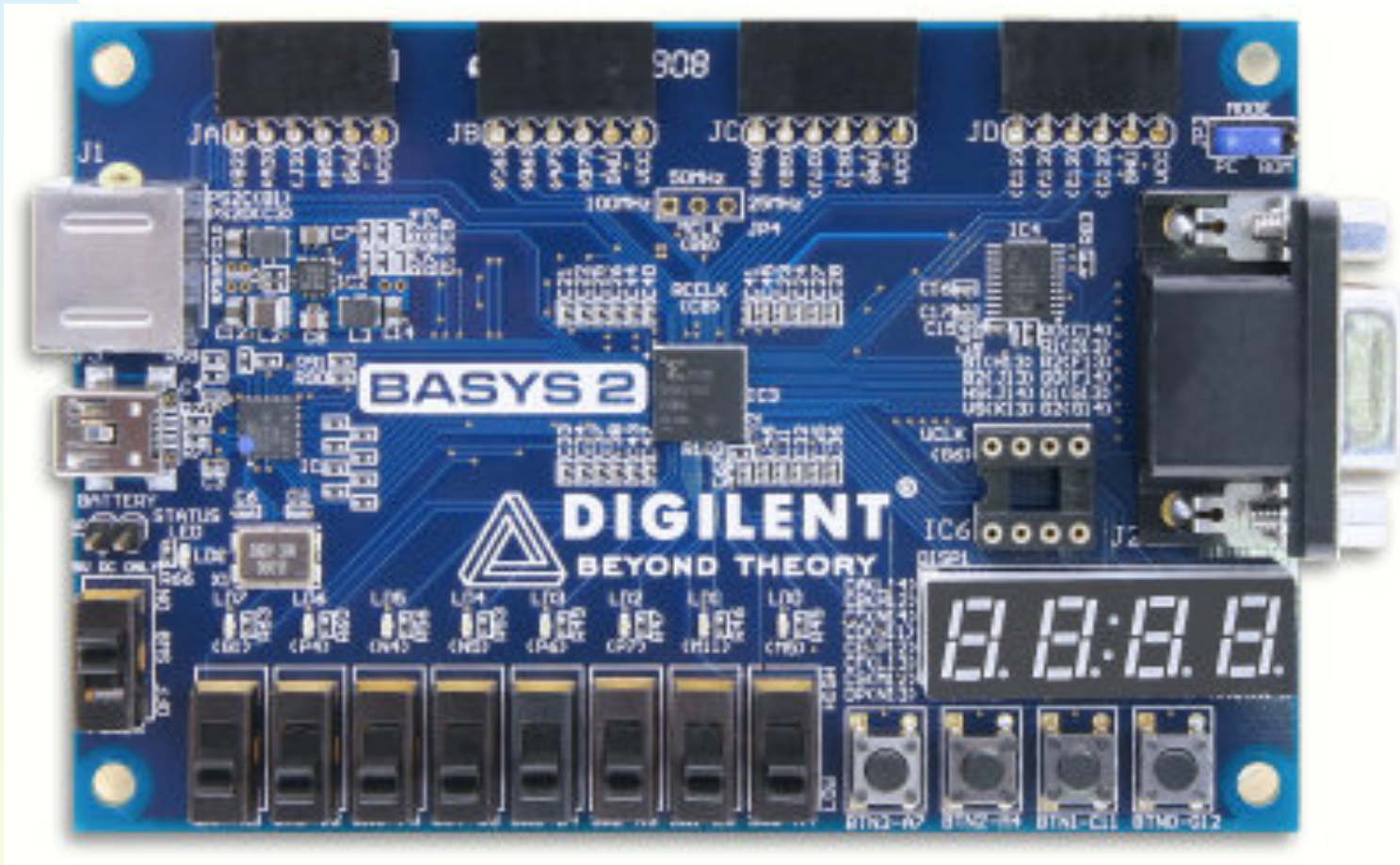
Architecture name

Port Name	Direction	Bus	MSB	LSB
a	in	<input type="checkbox"/>		
b	in	<input type="checkbox"/>		
q	out	<input type="checkbox"/>		
sel	in	<input type="checkbox"/>		
	in	<input type="checkbox"/>		
	in	<input type="checkbox"/>		
	in	<input type="checkbox"/>		
	in	<input type="checkbox"/>		
	in	<input type="checkbox"/>		
	in	<input type="checkbox"/>		

# Edit sources



# Target to your hardware



# Define constraints

The screenshot displays the Xilinx ISE software interface for an RTL Design. The main window shows a grid of the device (xc3s100ecp132-4) with various components placed on it. The 'RTL Netlist' window shows a hierarchy of components: mux\_2bit, Nets (4) (a, b, q, sel), and Primitives (1). The 'I/O Port Properties' window shows the configuration for the 'sel' port: Name: sel, Direction: Input, Site: A7, Package Pin: A7, and Fixed: checked. The 'I/O Ports' window shows a table of all ports:

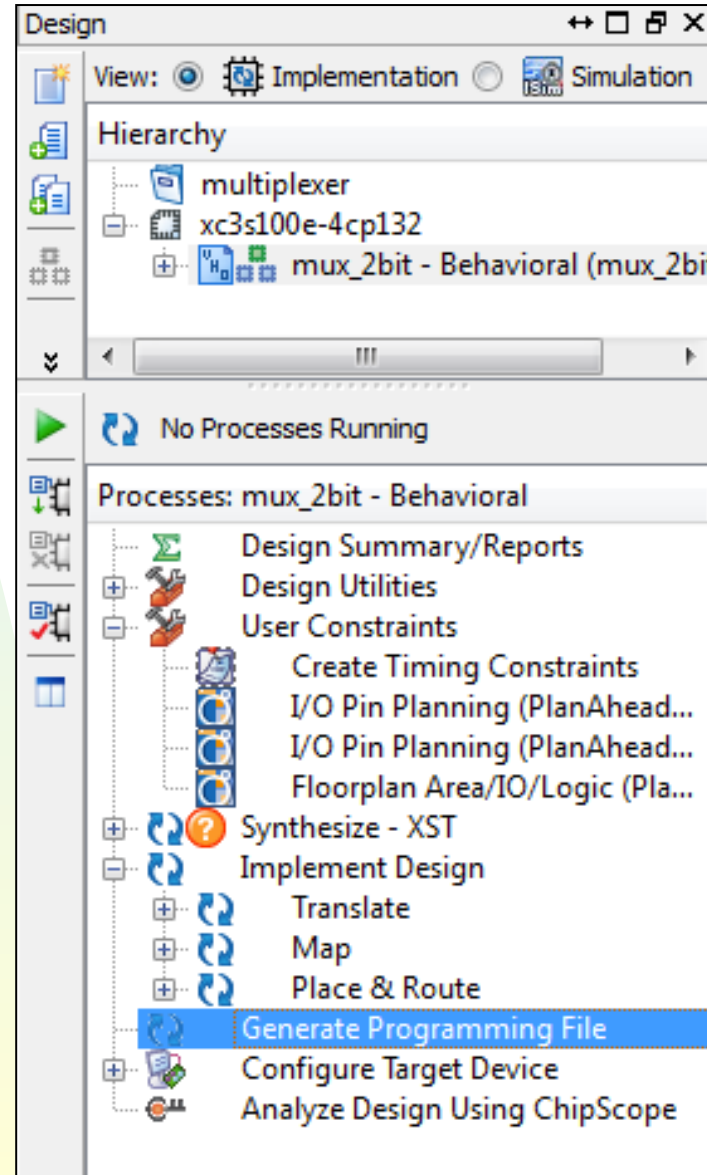
Name	Dir	Neg Diff Pair	Site	Bank	I/O Std	Vcco	Vref	Driv
All ports (4)								
Scalar ports (4)								
a	Input		P11	2	LVC MOS25	2.5		
b	Input		L3	3	LVC MOS25	2.5		
q	Output		M5	2	LVC MOS25	2.5		
sel	Input		A7	0	LVC MOS25	2.5		

In this case, only I/O needs to be declared. More complex designs also need info on timing constraints

# User Constraint File (UCF)

```
1  
2 # PlanAhead Generated physical constraints  
3  
4 NET "a" LOC = P11;  
5 NET "b" LOC = L3;  
6 NET "q" LOC = M5;  
7 NET "sel" LOC = A7;  
8
```

# Implement the design



ISE follows the design flow up to the selected point.



# Configure the FPGA

The screenshot displays the iMPACT software interface with the following components:

- IMPACT Flows:** A tree view on the left showing 'Boundary Scan' selected, with sub-items 'SystemACE', 'Create PROM File (PROM File Format...', and 'WebTalk Data'.
- IMPACT Processes:** A list of available operations including 'Program', 'Get Device ID', 'Get Device Signature/Usercode', 'Read Device Status', and 'One Step SVF'.
- Diagram:** A schematic showing two Xilinx devices connected in series. The first device is labeled 'xc3s100e mux\_2bit.bit' and has a 'TDI' input and 'TDO' output. The second device is labeled 'xcf02s bypass'. A dashed box labeled 'SPI/BPI ?' is positioned above the first device.
- Console:** A text area at the bottom showing the message: 'INFO:iMPACT:501 - '1': Added Device xc3s100e successfully.' followed by dashed lines.
- Status Bar:** Shows 'Configuration', 'Digilent Basys2-100', and '4000000'.